TEXAS INSTRUMENTS
ISO6163
SLLSFX1 – SEPTEMBER 2024

ISO6163 Low-Power, High-Speed Six-Channel Digital Isolator With Automatic Enable

ADVANCE INFORMATION

1 Features

- Pin-to-pin low power replacement for industry-standard six-channel digital isolators supporting high energy efficiency application requirements
- Automatic enable of high speed channels to support bi-directional wake up with ultra low quiescent current in STANDBY state: 442µA (maximum) current per side at V_{CC} = 3.3V (85°C)
- 50Mbps data rate on high-speed data channels
- 4Mbps data rate on low-speed control channels with automatic enable
- Low propagation delay: 13.75ns (maximum) at 3.3V
- Robust SiO_2 isolation barrier:
  - Wide temperature range: –40°C to 125°C
  - Up to 5000V_{RMS} isolation rating
  - Up to 10.4kV surge capability
  - ±50kV/µs typical CMTI
- Supply range: 2.5 to 5.5V
- 2.5 to 5.5V level translation
- Default output *high* (ISO6163) and *low* (ISO6163F) options
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- Appliances including high energy efficient products
- Electricity meter and Grid
- Power supplies
- Factory automation
- Building automation
- Lighting
- Motor drives

3 Description

The ISO6163 devices are high-performance, six-channel digital isolators designed for high energy efficiency and cost-sensitive applications requiring up to 5000V_{RMS} isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO6163 devices are optimized with low quiescent current and bi-directional automatic enable of the high speed data channels for use in high energy efficiency applications such as appliances, battery monitoring, metering and grid.

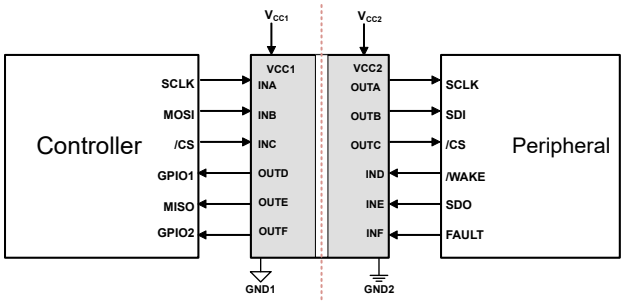
These devices are designed with low power consumption, high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital I/O signals such as: GPIOs, SPI (ADC, DAC, other peripherals), UART, RS-485, RS-232, and CAN . Each channel has a logic input and output buffer separated by TI's proprietary silicon dioxide (SiO_2) isolation barrier.

The ISO6163 device has three forward channels and three reverse-direction channels. This device provides two low speed data channels with bi-directional automatic enable control functionality. The low speed control channels automatically enable the high speed channels when needed or turn them off (outputs high impedance) to further reduce power consumption when high speed data transfer is not needed by the system. In the event of input power or signal loss, the default output level is *high* for devices without suffix F and *low* for devices with suffix F.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
ISO6163	DW (SOIC, 16)	10.30mm × 10.30mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

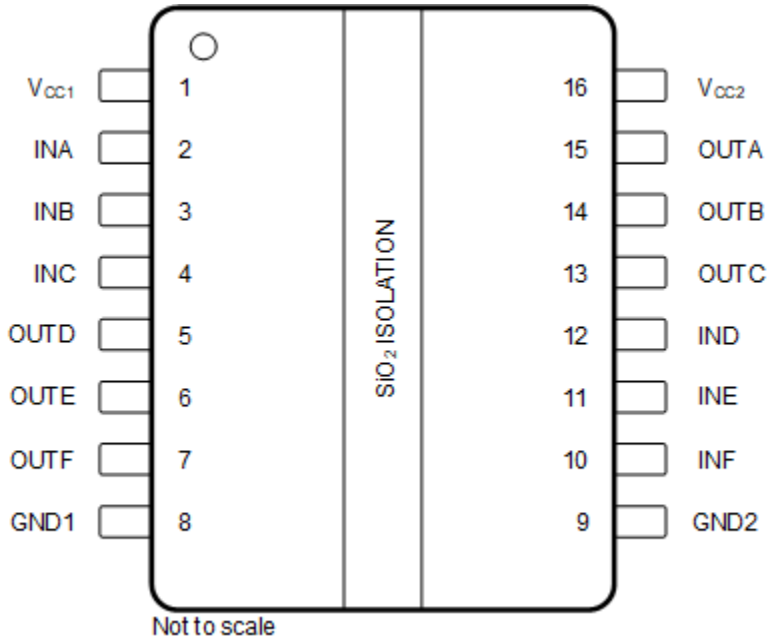

Figure 4-1. DW Package, 16-Pin Wide-SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CC1}	1	P	Power supply, side 1
INA	2	I	High-speed digital input, channel A
INB	3	I	High-speed digital input, channel B
INC	4	I	Low-speed control channel with automatic enable, channel C
OUTD	5	O	Digital output, channel D
OUTE	6	O	Digital output, channel E
OUTF	7	O	Digital output, channel F
GND1	8	GND	Ground connection for V_{CC2}, INA, INB, INC, OUTD, OUTE, and OUTF
GND2	9	GND	Ground connection for V_{CC2}, OUTA, OUTB, OUTC, IND, INE, and INF
INF	10	I	High-speed digital input, channel F
INE	11	I	High-speed digital input, channel E
IND	12	I	Low-speed control channel with automatic enable, channel D
OUTC	13	O	Digital output, channel C
OUTB	14	O	Digital output, channel B
OUTA	15	O	Digital output, channel A
V_{CC2}	16	P	Power supply, side 2

(1) I = input, O = output, P = power, GND = ground

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5 Specifications

5.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	6	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5(3)	
Output current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1		2.5		5.5	V
V_{CC2} (1)	Supply Voltage Side 2		2.5		5.5	V
Vcc (UVLO+)	UVLO threshold when supply voltage is rising				2.45	V
Vcc (UVLO-)	UVLO threshold when supply voltage is falling		2.09			V
Vhys (UVLO)	Supply voltage UVLO hysteresis			0.08		V
V_{IH}	High level Input voltage		0.7 x V_{CCI} (2)		V_{CCI} (2)	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI} (2)	V
I_{OH}	High level output current	V_{CCO} (2) = 5V	-4			mA
		V_{CCO} (2) = 3.3V	-4			mA
		V_{CCO} (2) = 2.5V	-2			mA
I_{OL}	Low level output current	V_{CCO} (2) = 5V			4	mA
		V_{CCO} (2) = 3.3V			4	mA
		V_{CCO} (2) = 2.5V			2	mA
DR	Data Rate for channels A, B, E, and F		0		50	Mbps
	Data Rate for channels C and D		0		4	
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

5.4 Thermal Information

THERMAL METRIC(1)		ISO616x DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 25MHz 50% duty cycle square wave			120	mW
P_{Dx}	Maximum power dissipation (side-1 or side-2)				60	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			16-DW	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	V_{IOSM} ≥ 1.3 x V_{IMP}; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10s	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	≅2.4	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1, IEC 61010-1 and IEC 60601	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =61.5°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			369	mA
		$R_{\theta JA}$ = 61.5°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			564	
		$R_{\theta JA}$ = 61.5°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			739	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 61.5°C/W, T_J = 150°C, T_A = 25°C			2032	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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5.9 Electrical Characteristics—5V Supply (±10%)

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA; See Figure 6-1	V_{CCO} - 0.4 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; See Figure 6-1			0.4	V
$V_{IT+(IN)}$	Rising input threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.04 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
I_{O_LP}	Low-Power mode output current			5		nA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V; See Figure 6-4	25	50		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC} + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 5V		1.7		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

5.10 Supply Current Characteristics—5V Supply (±10%)

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - STANDBY (Low Power)(1)	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC1}		0.375	0.478	mA
		–40°C to 85°C			0.375	0.460	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.385	0.495	
		–40°C to 85°C			0.385	0.475	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC2}		0.375	0.478	
		–40°C to 85°C			0.375	0.460	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.385	0.495	
		–40°C to 85°C			0.385	0.475	
Supply current - ACTIVE - DC signal (2)	V_I = V_{CC1} or V_I = 0V		I_{CC1}		1.3	1.72	
			I_{CC2}		1.3	1.72	
Supply current - ACTIVE - AC signal (2)	All channels switching with square wave clock inputs; C_L = 0pF	1Mbps	I_{CC1}		1.4	1.86	
			I_{CC2}		1.4	1.86	
	A, B, E, and F channels switching with square wave clock input; C and D channels switching at 4Mbps; C_L = 0pF	10Mbps	I_{CC1}		2.3	3.01	
			I_{CC2}		2.3	3.01	
		20Mbps	I_{CC1}		3.1	4.19	
			I_{CC2}		3.1	4.19	
		25Mbps	I_{CC1}		3.5	4.7	
			I_{CC2}		3.5	4.7	
		50Mbps	I_{CC1}		5.6	7.5	
			I_{CC2}		5.6	7.5	

(1) Supply current valid for both INC and IND HIGH for STANDBY state.
(2) Supply current valid for at least one of INC or IND LOW for ACTIVE state.

5.11 Electrical Characteristics—3.3V Supply (±10%)

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA; See Figure 6-1	V_{CCO} - 0.4 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; See Figure 6-1			0.4	V
$V_{IT+(IN)}$	Rising input threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.04 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
I_{O_LP}	Low-Power mode output current			3		nA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V; See Figure 6-4	25	50		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC} + 0.4×sin(2πft), f = 2MHz, V_{CC} = 3.3V		1.7		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

5.12 Supply Current Characteristics—3.3V Supply (±10%)

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - STANDBY (Low Power) (1)	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC1}		0.36	0.458	mA
		–40°C to 85°C			0.36	0.442	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.366	0.465	
		–40°C to 85°C			0.366	0.448	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC2}		0.36	0.458	
		–40°C to 85°C			0.36	0.442	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.366	0.465	
		–40°C to 85°C			0.366	0.448	
Supply current - ACTIVE - DC signal (2)	V_I = V_{CC1} or V_I = 0V		I_{CC1}		1.24	1.67	
			I_{CC2}		1.24	1.67	
Supply current - ACTIVE - AC signal (2)	All channels switching with square wave clock inputs; C_L = 0pF	1Mbps	I_{CC1}		1.31	1.77	
			I_{CC2}		1.31	1.77	
	A, B, E, and F channels switching with square wave clock input; C and D channels switching at 4Mbps; C_L = 0pF	10Mbps	I_{CC1}		2.03	2.7	
			I_{CC2}		2.03	2.7	
		20Mbps	I_{CC1}		2.75	3.64	
			I_{CC2}		2.75	3.64	
		25Mbps	I_{CC1}		3.06	4.06	
			I_{CC2}		3.06	4.06	
		50Mbps	I_{CC1}		4.73	6.3	
			I_{CC2}		4.73	6.3	

(1) Supply current valid for both INC and IND HIGH for STANDBY state.
(2) Supply current valid for at least one of INC or IND LOW for ACTIVE state.

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5.13 Electrical Characteristics—2.5V Supply (Minimum)

V_{CC1} = V_{CC2} = 2.5V min (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA; See Figure 6-1	V_{CCO} - 0.4 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; See Figure 6-1			0.4	V
$V_{IT+(IN)}$	Rising input threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.04 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
I_{O_LP}	Low-Power mode output current			2.2		nA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V; See Figure 6-4	25	50		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC} + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		1.7		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

5.14 Supply Current Characteristics—2.5V Supply (Minimum)

V_{CC1} = V_{CC2} = 2.5V min (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - STANBDY (Low Power) (1)	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC1}		0.35	0.448	mA
		–40°C to 85°C			0.35	0.432	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.356	0.455	
		–40°C to 85°C			0.356	0.438	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = VCC_I on channels A, B, E, F (default level).	–40°C to 125°C	I_{CC2}		0.35	0.448	
		–40°C to 85°C			0.35	0.432	
	Device in STANDBY state. V_I = VCC_I on channels C and D (default level). V_I = 0V on channels A, B, E, F.	–40°C to 125°C			0.356	0.455	
		–40°C to 85°C			0.356	0.438	
Supply current - ACTIVE - DC signal (2)	V_I = V_{CC1} or V_I = 0V		I_{CC1}		1.23	1.65	
			I_{CC2}		1.23	1.65	
Supply current - ACTIVE - AC signal (2)	All channels switching with square wave clock inputs; C_L = 0pF	1Mbps	I_{CC1}		1.29	1.73	
			I_{CC2}		1.29	1.73	
	A, B, E, and F channels switching with square wave clock input; C and D channels switching at 4Mbps; C_L = 0pF	10Mbps	I_{CC1}		1.9	2.5	
			I_{CC2}		1.9	2.5	
		20Mbps	I_{CC1}		2.53	3.28	
			I_{CC2}		2.53	3.28	
		25Mbps	I_{CC1}		2.79	3.62	
			I_{CC2}		2.79	3.62	
		50Mbps	I_{CC1}		4.22	5.46	
			I_{CC2}		4.22	5.46	

(1) Supply current valid for both INC and IND HIGH for STANDBY state.
(2) Supply current valid for at least one of INC or IND LOW for ACTIVE state.

5.15 Switching Characteristics—5V Supply (±10%)

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Channels A, B, E, and F. See Figure 6-1		9	12	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	ns
t_{PLH}, t_{PHL}	Propagation delay time	Channels C and D. See Figure 6-1		9	12	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Channels A and B or E and F (consecutive channels in active mode)			1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	ns
t_r	Output signal rise time	See Figure 6-1		2.0	3.5	ns
t_f	Output signal fall time			2.0	3.5	ns
t_{LP_EN}	STANDBY State (low power) enable delay time	Time required transition to STANDBY state once channels C and D are in the inactive and HIGH states. See Figure 6-2	700	1000	1400	ms
t_{AMS}	ACTIVE sample time (portion of t_{LP_EN}), either C or D going LOW	ACTIVE sample deglitch time for STANDBY state enable delay time. See Figure 6-2	10		28	µs
t_{LPN}	STANDBY to ACTIVE (Low power to normal) transition time		20		52	µs
$t_{PU\_HS\_CH}$	Time from UVLO to valid output data on channels A, B, E, and F				120	µs
$t_{PU\_LS\_CH}$	Time from UVLO to valid output data on channels C and D				100	µs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 2.2V if the remaining device signals require normal mode operation. See Figure 6-3			13.5	µs
TIE	Time Interval Error	Channels A, B, E, and F. 2^{16} – 1 PRBS data at 50Mbps		0.08	2	ns
		Channels C and D. 2^{16} – 1 PRBS data at 4Mbps		0.12	2	ns
$t_{JIT(RJ)}$	Random jitter				1	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.16 Switching Characteristics—3.3V Supply (±10%)

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Channels A, B, E, and F. See Figure 6-1		9.6	13.75	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	ns
t_{PLH}, t_{PHL}	Propagation delay time	Channels C and D. See Figure 6-1		9.6	13.75	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Channels A and B or E and F (consecutive channels in active mode)			1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time	See Figure 6-1		2.1	3.5	ns
t_f	Output signal fall time			2.1	3.5	ns
t_{LP_EN}	STANDBY State (low power) enable delay time	Time required transition to STANDBY state once channels C and D are in the inactive and HIGH states. See Figure 6-2	700	1000	1400	ms
t_{AMS}	ACTIVE sample time (portion of t_{LP_EN}), either C or D going LOW	ACTIVE sample deglitch time for STANDBY state enable delay time. See Figure 6-2	10		28	µs
t_{LPN}	STANDBY to ACTIVE (Low power to normal) transition time		20		52	µs
$t_{PU\_HS\_CH}$	Time from UVLO to valid output data on channels A, B, E, and F				120	µs
$t_{PU\_LS\_CH}$	Time from UVLO to valid output data on channels C and D				100	µs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 2.2V if the remaining device signals require normal mode operation. See Figure 6-3			13.5	µs
TIE	Time Interval Error	Channels A, B, E, and F. 2^{16} – 1 PRBS data at 50Mbps		0.06	2	ns
		Channels C and D. 2^{16} – 1 PRBS data at 4Mbps		0.12	2	ns
$t_{JIT(RJ)}$	Random jitter				1	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.17 Switching Characteristics—2.5V Supply (Minimum)

V_{CC1} = V_{CC2} = 2.5V min (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Channels A, B, E, and F. See Figure 6-1		11	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	ns
t_{PLH}, t_{PHL}	Propagation delay time	Channels C and D. See Figure 6-1		11	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Channels A and B or E and F (consecutive channels in active mode)			1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time	See Figure 6-1		2.2	4.1	ns
t_f	Output signal fall time			2.2	4.1	ns
t_{LP_EN}	STANDBY State (low power) enable delay time	Time required transition to STANDBY state once channels C and D are in the inactive and HIGH states. See Figure 6-2	700	1000	1400	ms
t_{AMS}	ACTIVE sample time (portion of t_{LP_EN}), either C or D going LOW	ACTIVE sample deglitch time for STANDBY state enable delay time. See Figure 6-2	10		28	µs
t_{LPN}	STANDBY to ACTIVE (Low power to normal) transition time		20		52	µs
$t_{PU\_HS\_CH}$	Time from UVLO to valid output data on channels A, B, E, and F				120	µs
$t_{PU\_LS\_CH}$	Time from UVLO to valid output data on channels C and D				100	µs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 2.2V if the remaining device signals require normal mode operation. See Figure 6-3			13.5	µs
TIE	Time Interval Error	Channels A, B, E, and F. 2^{16} – 1 PRBS data at 50Mbps		0.06	2	ns
		Channels C and D. 2^{16} – 1 PRBS data at 4Mbps		0.13	2	ns
$t_{JIT(RJ)}$	Random jitter				1	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

5.18 Insulation Characteristics Curves

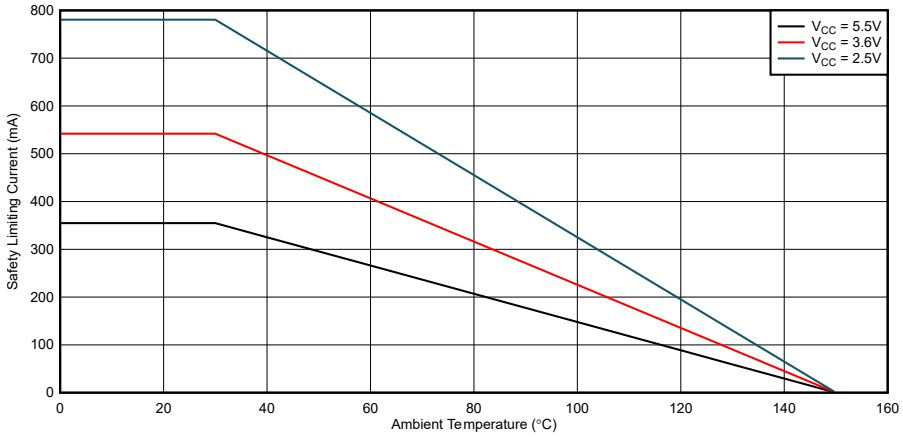


Figure 5-1. Thermal Derating Curve for Safety Limiting Current (mA) for DW-16 Package

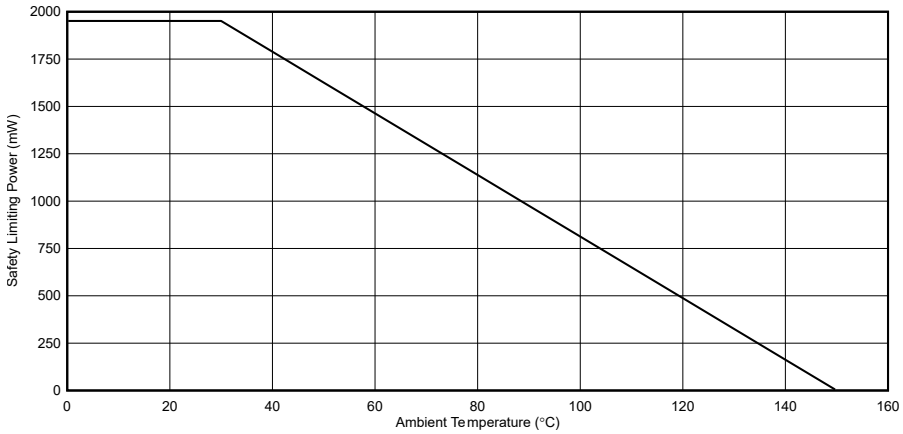


Figure 5-2. Thermal Derating Curve for Safety Limiting Power (mW) for DW-16 Package

ADVANCE INFORMATION

5.19 Typical Characteristics

5.19.1 Typical Characteristics: Supply Current ACTIVE state

ACTIVE state is forced with one low-speed control channel held LOW, the high-speed data and second low-speed control channel data rate is swept per the chart. Once the data-rate reaches 4Mbps, the second low-speed control channel data rate is held at 4Mbps as the high-speed data channels continue to rise until 50Mbps.

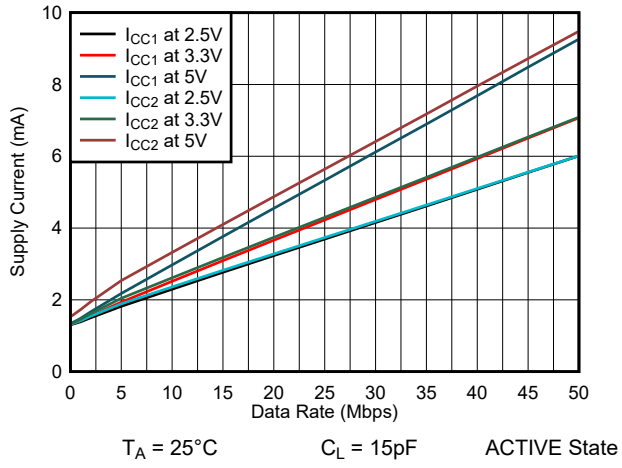


Figure 5-3. ISO6163 Supply Current vs Data Rate (With 15pF Load) for ACTIVE State

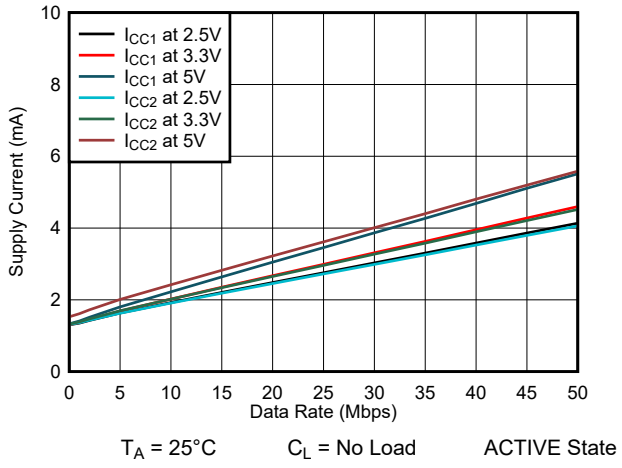
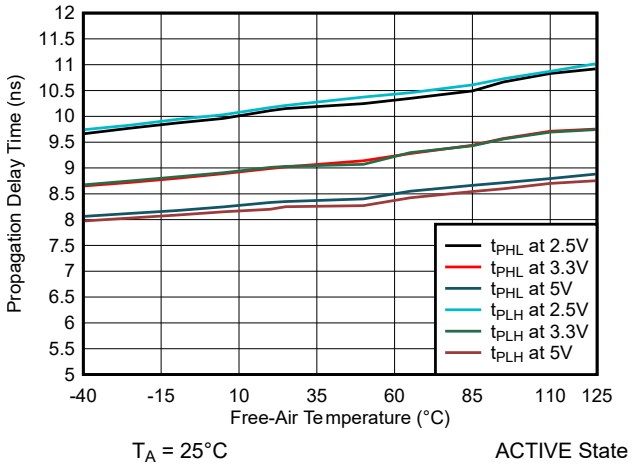


Figure 5-4. ISO6163 Supply Current vs Data Rate (With 15pF Load) for ACTIVE State

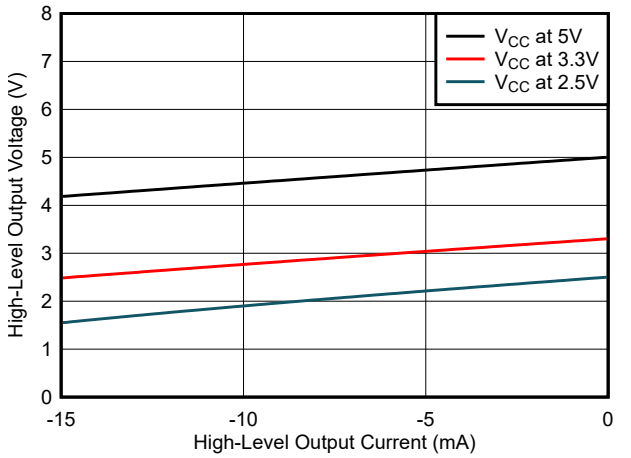
ADVANCE INFORMATION

5.19.2 Typical Characteristics: High-Speed Channels (ACTIVE state)



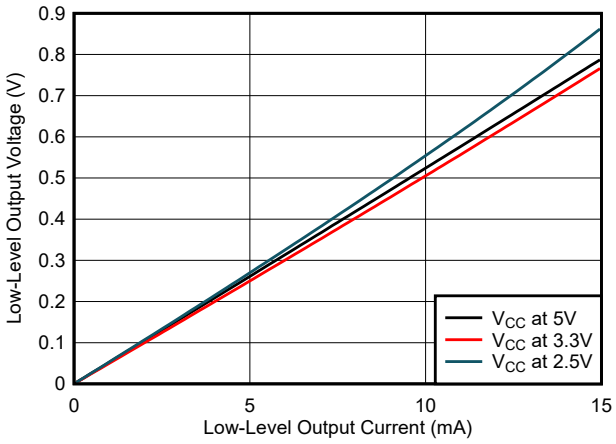
T_A = 25°C ACTIVE State

Figure 5-5. ISO6163 Propagation Delay Time vs Free-Air Temperature for High-Speed Channel



T_A = 25°C ACTIVE State

Figure 5-6. ISO6163 High-Level Output Voltage vs High-level Output Current for High-Speed Channel



T_A = 25°C ACTIVE State

Figure 5-7. ISO6163 Low-Level Output Voltage vs Low-Level Output Current for High-Speed Channel

5.19.3 Typical Characteristics: Supply Current STANDBY State

STANDBY state is held with one low-speed control channel held HIGH while second channel is swept. The data rates swept are selected to avoid LOW durations longer than t_{AMS} which transition the device to ACTIVE state.

Note

The high-speed channels are turned off (high impedance) in the device STANDBY state.

Note

For I_{CC1} and I_{CC2} at with DC signals on the low-speed control channels, please refer to the Supply Characteristics table for the supply voltage, V_{CC1} and V_{CC2}, supplied to each side of the isolator.

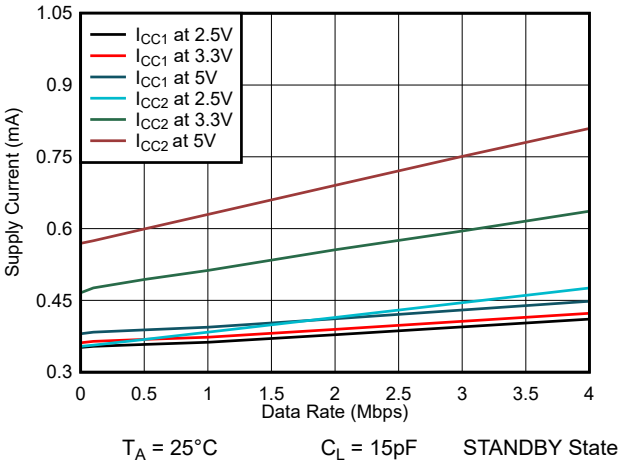


Figure 5-8. ISO6163 Supply Current vs Data Rate (With 15pF Load) for Low-Speed Channel in STANDBY state

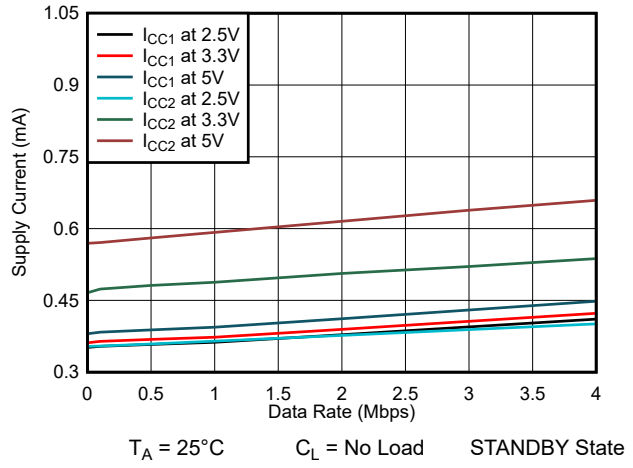


Figure 5-9. ISO6163 Supply Current vs Data Rate (With No Load) for Low-Speed Channel in STANDBY state

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5.19.4 Typical Characteristics: Low-Speed Control Channels (ACTIVE and STANDBY States)

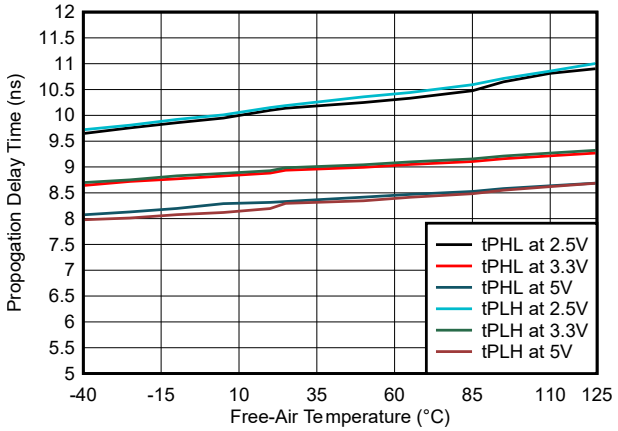
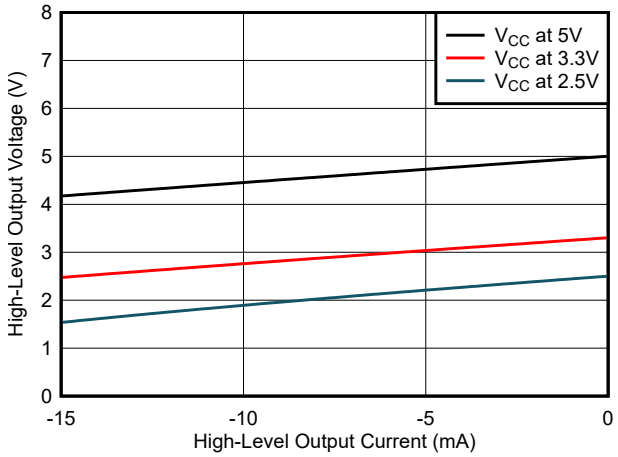
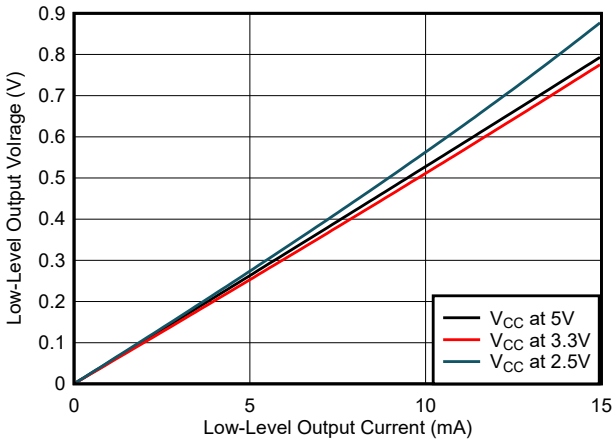


Figure 5-10. ISO6163 Propagation Delay Time vs Free-Air Temperature for Low-Speed Control Channel



T_A = 25°C

Figure 5-11. ISO6163 High-Level Output Voltage vs High-level Output Current for Low-Speed Control Channel



T_A = 25°C

Figure 5-12. ISO6163 Low-Level Output Voltage vs Low-Level Output Current for Low-Speed Control Channel

5.19.5 Typical Characteristics: Undervoltage Threshold

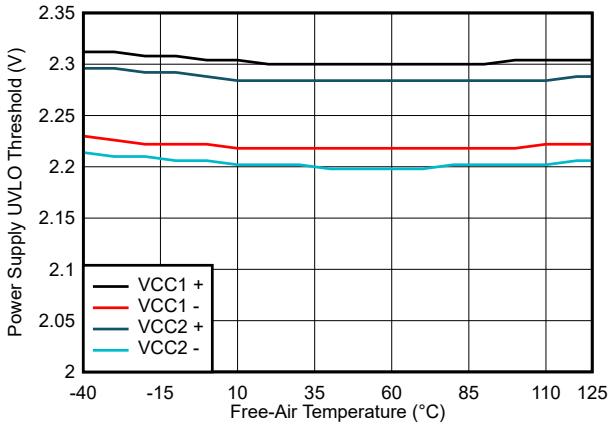


Figure 5-13. ISO6163 Power Supply Undervoltage Threshold vs Free-Air Temperature

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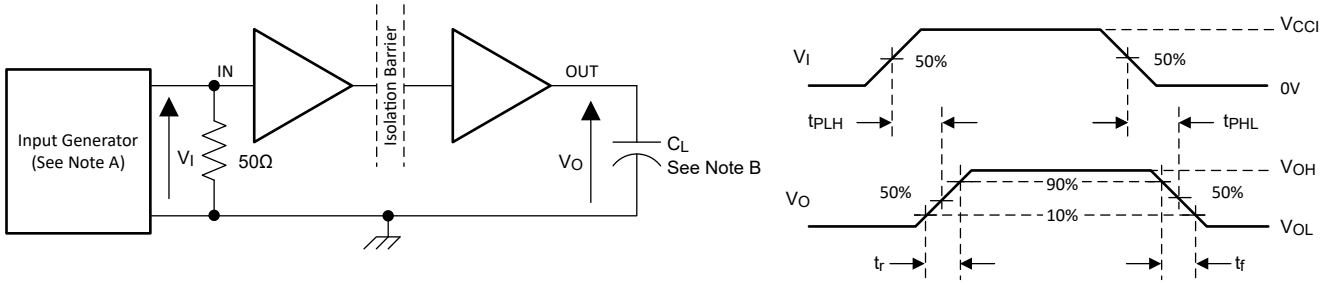
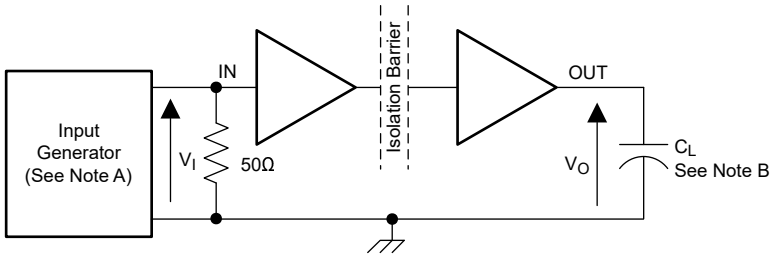
6 Parameter Measurement Information

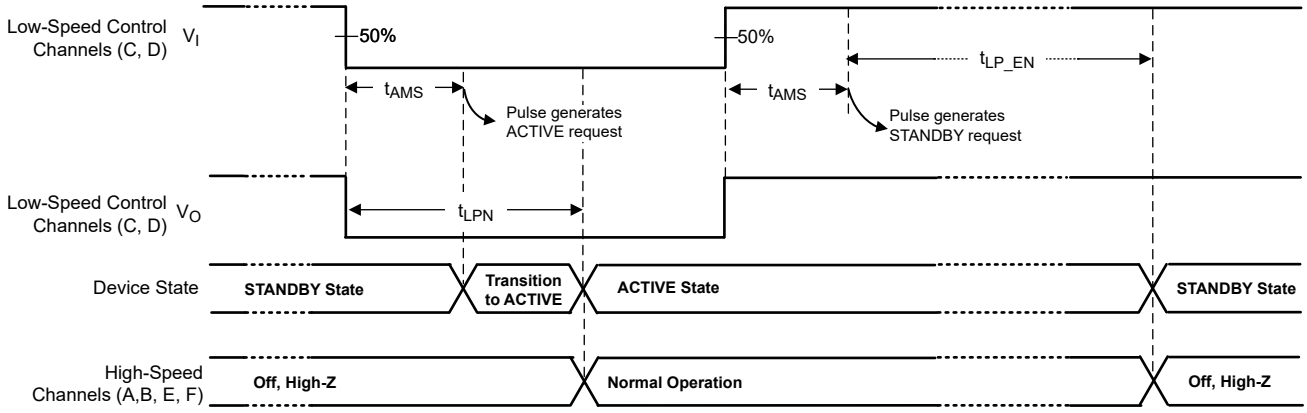


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms





A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

C. Low-Speed Control Channel not under test has a HIGH input.

Figure 6-2. Low-Speed Control Channel Automatic Enable Time Test Circuit and Waveform

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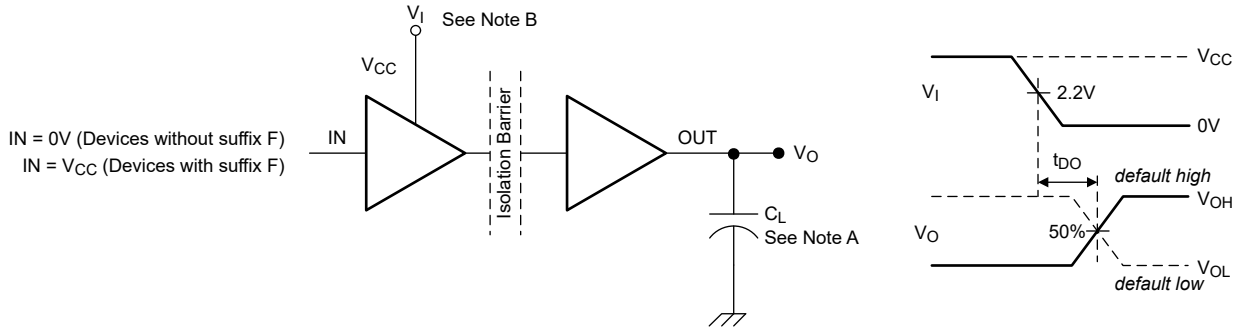
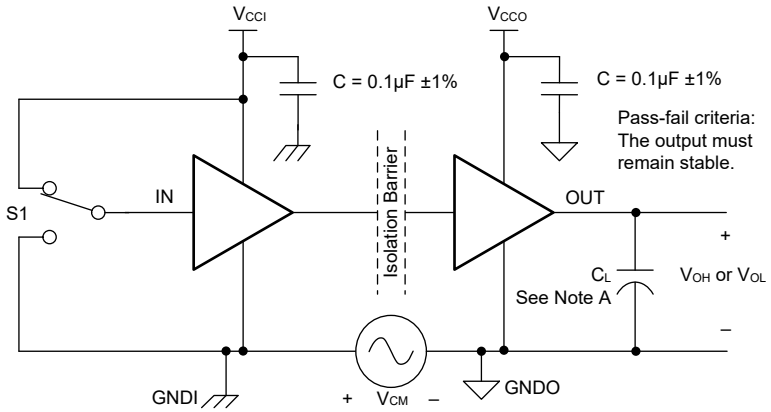


A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.
B. Power Supply Ramp Rate = 10mV/ns

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

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7 Detailed Description

7.1 Overview

The ISO6163 family of devices transmit digital data across a silicon dioxide based isolation barrier.

The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

The conceptual block diagram of the digital isolator, Conceptual Block Diagram of a Digital Isolator, shows a functional block diagram of a typical channel.

7.1.1 Functional Block Diagram

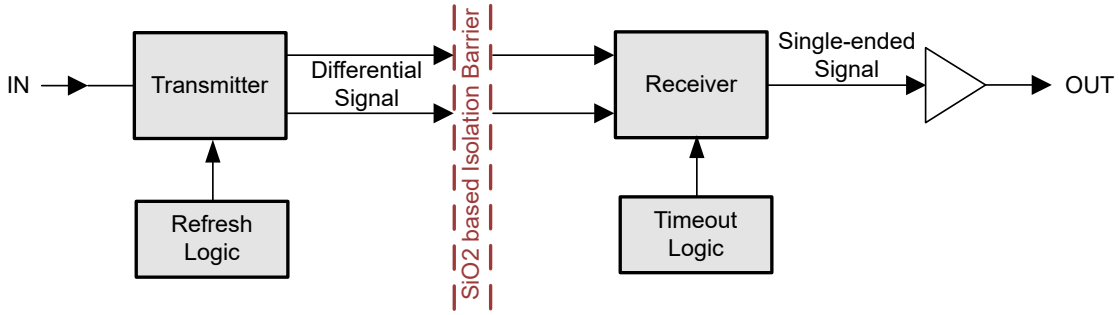

Figure 7-1. Conceptual Block Diagram of a Digital Isolator

7.1.2 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION		MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE
ISO6163	Forward	2 High-Speed	50Mbps	HIGH	Wide-SOIC (DW-16)
		1 Low-Speed Control with Automatic Enable	4Mbps (1)		
	Reverse	2 High-Speed	50Mbps		
		1 Low-Speed Control with Automatic Enable	4Mbps (1)		

(1) Up to 4Mbps when one low-speed control channel held low, or up to 35kbps when both low-speed control channels used for data. Data rates when both channels are used for data are limited by the data, protocol plus the t_{AMS} ACTIVE sample time and t_{LP_EN} STANDBY state enable delay time.

7.2 High-Speed Data Channels: A, B, E and F

The ISO6163 family of devices have four high-speed data channels used for clocking, data and other high data rate requirements in the system. These high-speed channels are enabled in the device ACTIVE state and turned off (high impedance) in the device STANDBY state. The device state is determined by the low-speed control channels C and D with automatic enable.

7.3 Low-Speed Control Channels With Automatic Enable: C and D

The ISO6163 family of devices have two low-speed control channels (C and D channels), one in each direction, with automatic enable. These two channels control the entry and exit from STANDBY state (low power, high-speed channels turned off and high impedance) and ACTIVE state (normal operation) of the device. With one automatic enable channel in each direction, the ISO6163 device supports power up and down control in both directions such that a host MCU (SPI NCS for example) or peripheral (NINT for example) wakes up the device and system.

Table 7-2. Device States based on Low-Speed Control Channels with Automatic Enable

INC	IND	Device State	Comment
HIGH	HIGH	STANDBY (Low Power)	INC and IND both HIGH enables STANDBY state (low power). STANDBY is only enabled when INC and IND are static HIGH with no activity or LOW on either of the channels for longer than t_{AMS} monitoring window and after the STANDBY low power reaction time t_{LP_EN}. High-speed channels A, B, E and F are high impedance.
LOW	LOW	ACTIVE (Normal Operation)	INC and IND both LOW enables all channels for ACTIVE state (normal operation).
LOW	HIGH	ACTIVE (Normal Operation)	INC LOW enables all channels for ACTIVE state (normal operation).
HIGH	LOW	ACTIVE (Normal Operation)	IND LOW enables all channels for ACTIVE state (normal operation).

7.3.1 Low-Speed Control Channels: Timing and Level Details for Automatic Enable

The low-speed control channels with automatic enable have ACTIVE state sample time and delay timer to prevent unintended entry to or exit from STANDBY state. This section explains the impact of these timing requirements on the automatic enable functionality and the maximum data rate possible in the low-speed control channels.

Both low-speed control channels, C and D, have an ACTIVE sample time, t_{AMS}, preventing noise from triggering state transitions. When at least one of the low-speed control channels, C and D, is LOW longer than the ACTIVE sample time, the device generates an ACTIVE mode request and either transitions to ACTIVE state or remains in ACTIVE state, canceling any STANDBY requests that can be generated. When the device must transition from STANDBY to ACTIVE upon an ACTIVE request, the device does so within t_{LPN} from the falling edge on one or both of the low-speed control channels.

When both low-speed control channels have been HIGH longer than the ACTIVE sample time a STANDBY request is generated. As long as an ACTIVE mode request is not generated before the STANDBY state enable delay time, t_{LP_EN}, elapses the device transitions to STANDBY state and remains there until an ACTIVE node request is generated.

The following flowchart and figures show how the ACTIVE sample time, STANDBY state enable delay time and power up conditions impact the state of the device and the high-speed channels.

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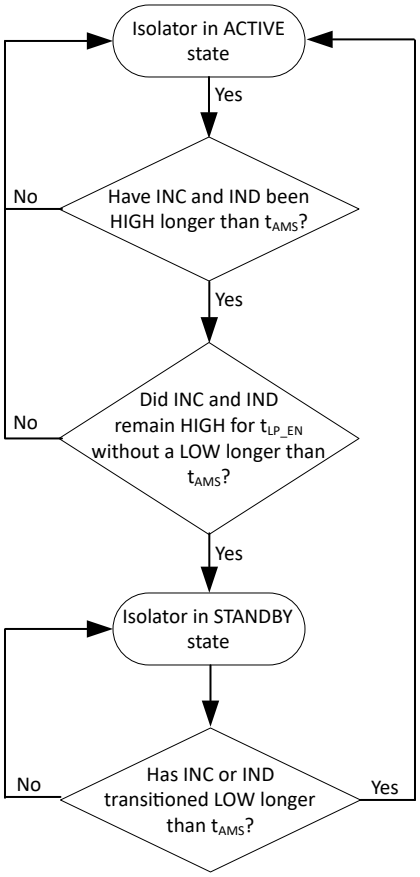


Figure 7-2. Low-Speed Control Channel Automatic Enable State Changes Flowchart

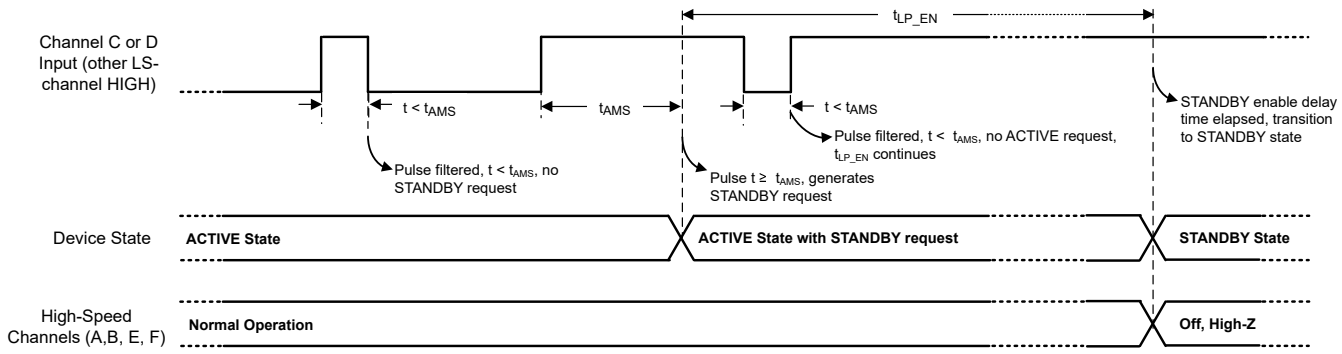


Figure 7-3. Low-Speed Control Channel Automatic Enable, Case 1 (ACTIVE to STANDBY Example)

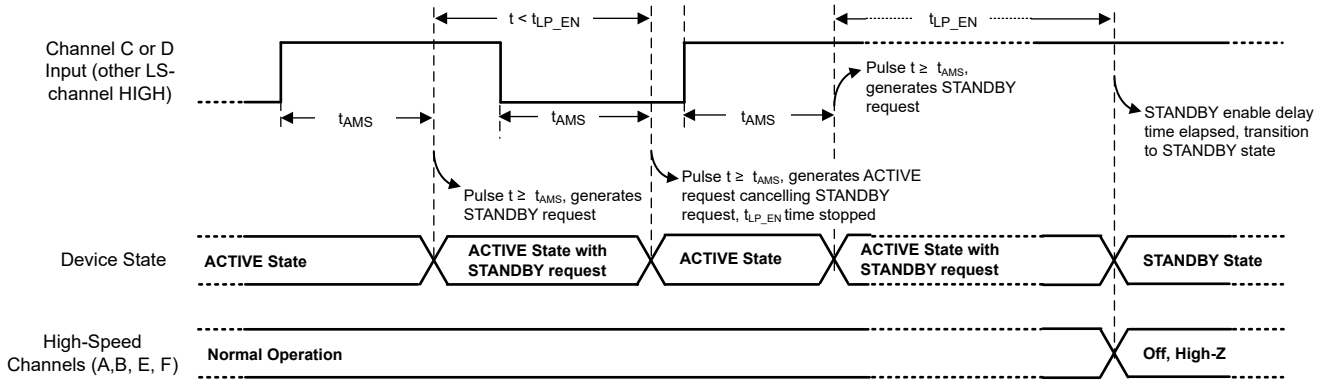


Figure 7-4. Low-Speed Control Channel Automatic Enable, Case 2 (ACTIVE to STANDBY Example With One Canceled STANDBY Request)

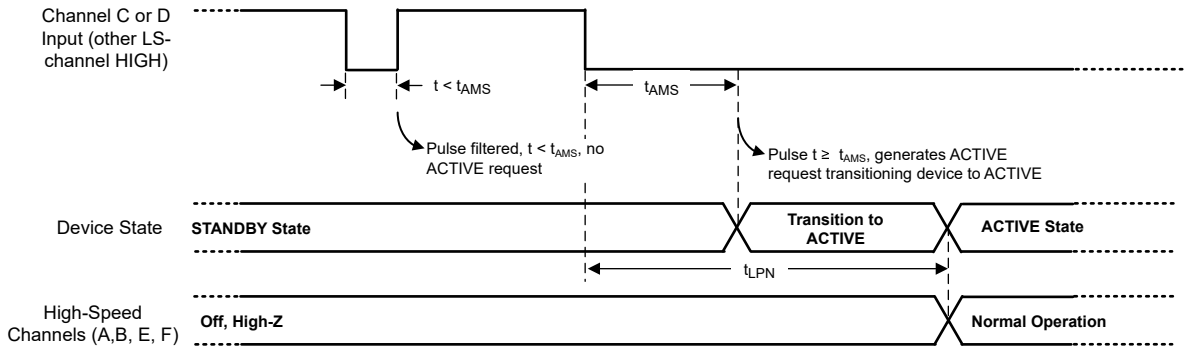


Figure 7-5. Low-Speed Control Channel Automatic Enable, Case 3 (STANDBY to ACTIVE Example With One Canceled STANDBY Request)

7.3.2 Low-Speed Control Channels: Considerations if Used for Data

If the low-speed data channels are used for data, the design must consider the impact of the automatic enable timing with respect to the data rate and protocol used for data to avoid unintentional device state changes.

The ACTIVE state sample time, t_{AMS}, limits the maximum data rate that can be used in the low-speed control signals.

In ACTIVE state, if at least one of the channels is held LOW, then the full data rate in the second low-speed control channel is usable. However if both channels are switching, the design must verify that at least one of the low-speed channels has a LOW longer than t_{AMS} before the minimum STANDBY state enable delay time, $_{LP\_EN}$ elapses to prevent the device from unintentionally transitioning to STANDBY state.

In STANDBY state, any data rate and protocol combination generating a LOW longer than t_{AMS} generate an ACTIVE request and transition the device to ACTIVE state.

7.3.3 Low-Speed Control Channels: Considerations During Power Up and Device Reset Events

The device takes $t_{PU\_LS\_CH}$ time to power up from any un-powered or brownout condition below the UVLO threshold until the low-speed control channel outputs to become valid and $t_{PU\_LS\_CH}$ time for the high-speed data channel outputs to be become valid.

During device power up or recovery from any reset or UVLO condition if ACTIVE state is desired, at least one of the low-speed control channels must be held LOW longer than the ACTIVE sample time, t_{AMS}, after $t_{PU\_LS\_CH}$ to stay in ACTIVE state, or the device transitions to STANDBY state after t_{LP_EN} time. See Section 7.3.2 for details on data use impact on device states.

ADVANCE INFORMATION

7.4 Device Functional Modes

Table 7-3 lists the functional modes for the ISO6163 devices.

Table 7-3. Function Table

V_{CCI} (1)	V_{CCO}	Low-Speed Control INPUT (INB, INC)	Low-Speed OUTPUT (OUTC, OUTD)	High-Speed INPUT (INA, INB, INE, INF) (3)	High-Speed OUTPUT (OUTA, OUTB, OUTE, OUTF)	COMMENTS
PU	PU	at least one L	Output mirrors input	H	H	ACTIVE (Normal Operation): A channel output, OUTx, is the same as the logic state of the corresponding input,INx.
				L	L	
				Open	Default	ACTIVE (Default mode): When INx is open, the corresponding channel output, OUTx, is at the default logic state. Default is *High* for ISO6163 and *Low* for ISO6163 with F suffix.
PU	PU	Both H or open	Output mirrors input	X	Z	STANDBY (Low Power): A HIGH value of both low-speed control channels cause the high-speed channel outputs to be high-impedance.
PD	PU	X	Default	X	Default	Default mode: When V_{CCI} is unpowered, a channel output, OUTx, goes to the logic state based on the selected default option. Default is *High* for ISO6163 and *Low* for ISO6163 with F suffix. When V_{CCI} transitions from unpowered to powered-up, the channel output, OUTx, goes to the same logic state of the corresponding input, INx. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output, OUTx, goes to the same logic state of the corresponding input, INx.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.45V); PD = Powered down (V_{CC} ≤ 2.09V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
(2) The outputs are in undetermined state when 2.09V < V_{CCI}, V_{CCO} < 2.45V
(3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output

7.4.1 Device I/O Schematics

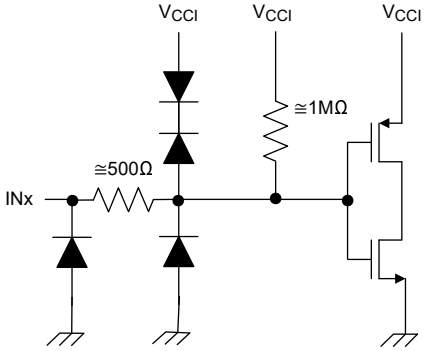


Figure 7-6. Device Input Schematic (Without F Suffix)

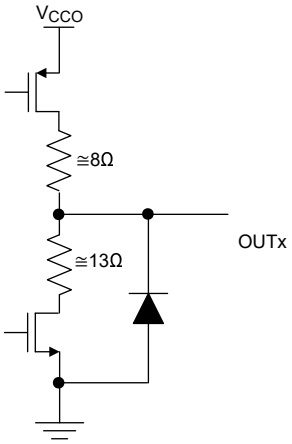


Figure 7-7. Device Output Schematic

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO6163 devices are high-performance, six-channel digital isolators. These devices come with 4 high-speed channels and two low-speed control channels with automatic enable controlling the high-speed outputs in normal or low-power modes. The ISO6163 devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.5V to 5.5V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions allowing the device to provide level shifting in addition to isolation. As an example, supplying the ISO6163 V_{CC1} with 3.3V (which is within 2.5V to 5.5V) and V_{CC2} with 5V (which is also within 2.5V to 5.5V) is possible. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

Figure 8-1 shows the isolated serial peripheral interface (SPI).

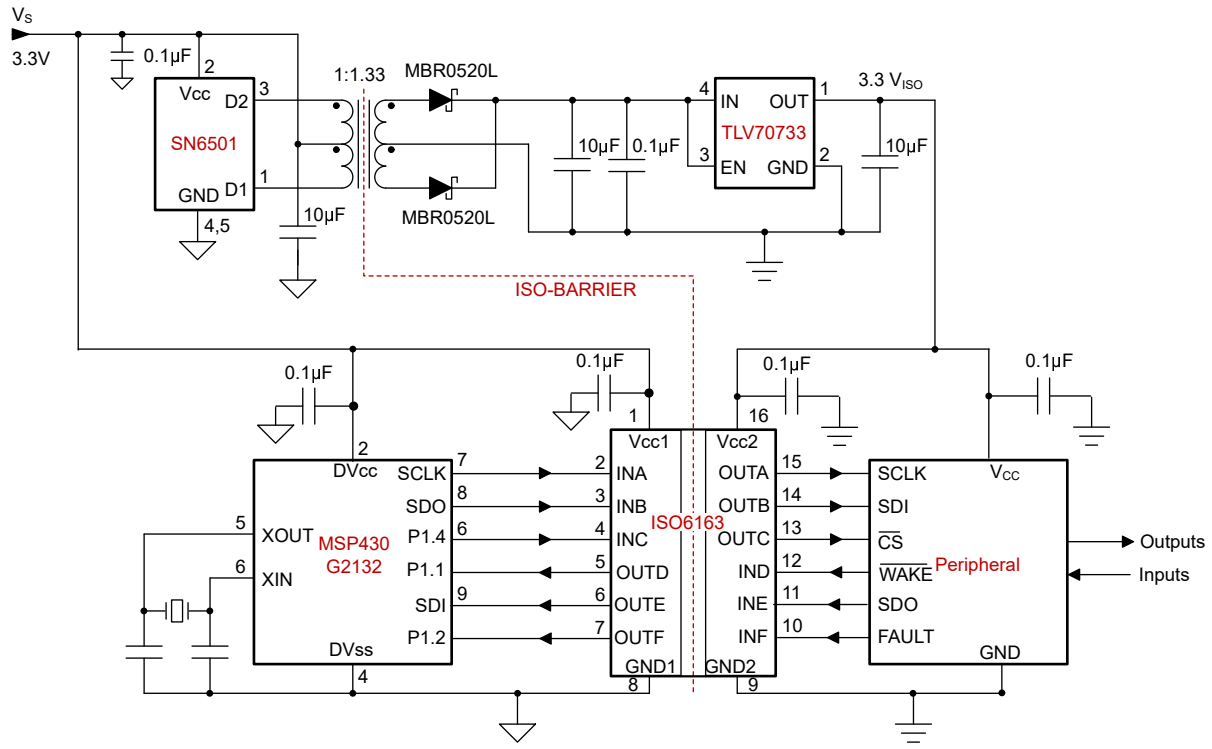


Figure 8-1. Isolated SPI With Automatic Enable for an Isolated Peripheral With Wake Up

ADVANCE INFORMATION

8.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.5V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO6163 family of devices only require two external bypass capacitors to operate.

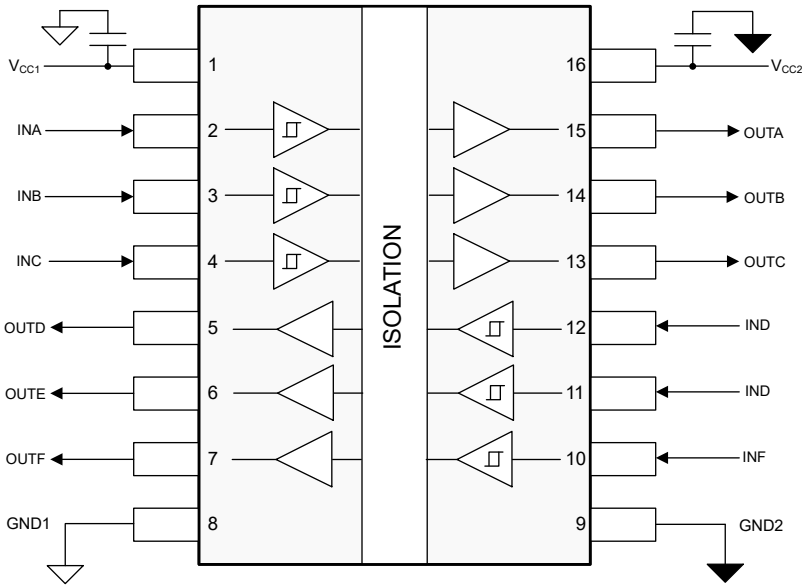
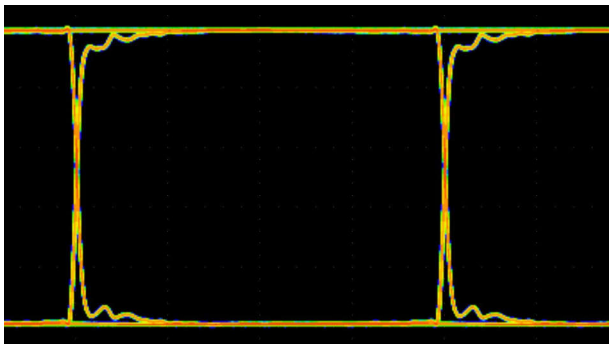


Figure 8-2. Typical ISO6163 Circuit Hook-up

ADVANCE INFORMATION

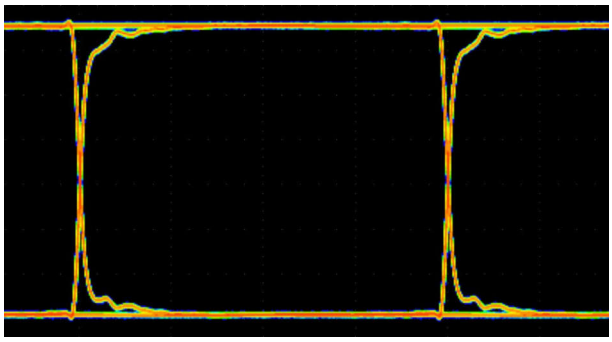
8.2.3 Application Curves

The following typical eye diagrams of the ISO6163 family of devices indicates low jitter and wide open eye at the maximum data rate of 50Mbps for the high-speed channels.



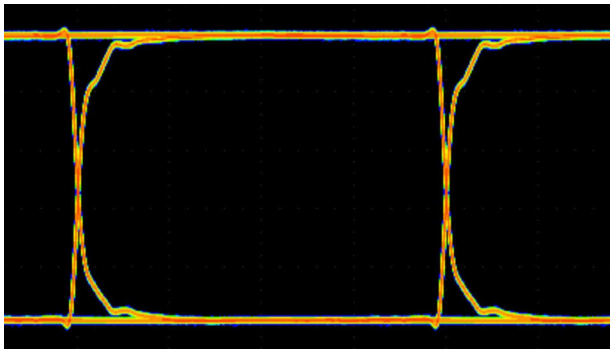
Horizontal 5ns / division, Vertical 1V / division.

Figure 8-3. High-Speed Channel Eye Diagram at 50Mbps PRBS 2^{16} – 1, 5V and 25°C



Horizontal 5ns / division, Vertical 0.5V / division.

Figure 8-4. High-Speed Channel Eye Diagram at 50Mbps PRBS 2^{16} – 1, 3.3V and 25°C



Horizontal 5ns / division, Vertical 0.5V / division.

Figure 8-5. High-Speed Channel Eye Diagram at 50Mbps PRBS 2^{16} – 1, 2.5V and 25°C

ADVANCE INFORMATION

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies* .

8.4 Layout

8.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Figure 8-7). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the related parasitic inductance) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane to the stack keeping the layers symmetrical. This makes the stack mechanically stable and prevents warping. The power and ground plane of each power domain can be placed closer together, thus increasing the high-frequency bypass capacitance.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating below 150Mbps, (or rise and fall times higher than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

8.4.2 Layout Example

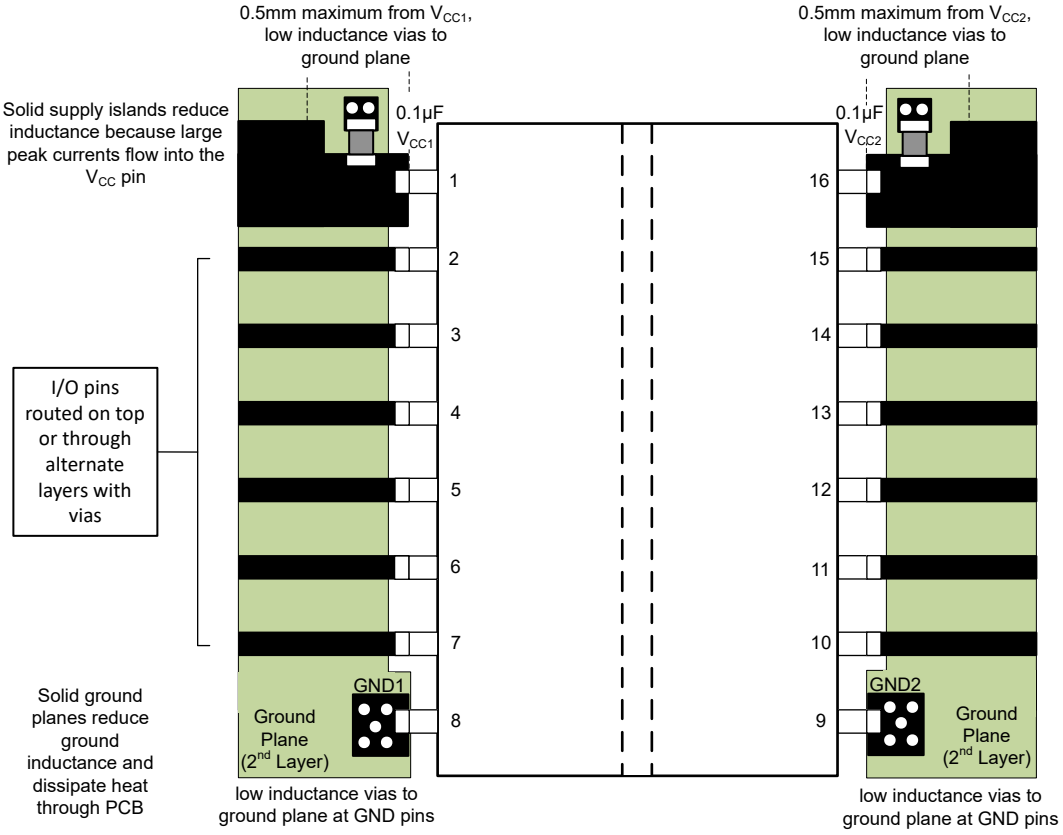


Figure 8-6. Layout Example

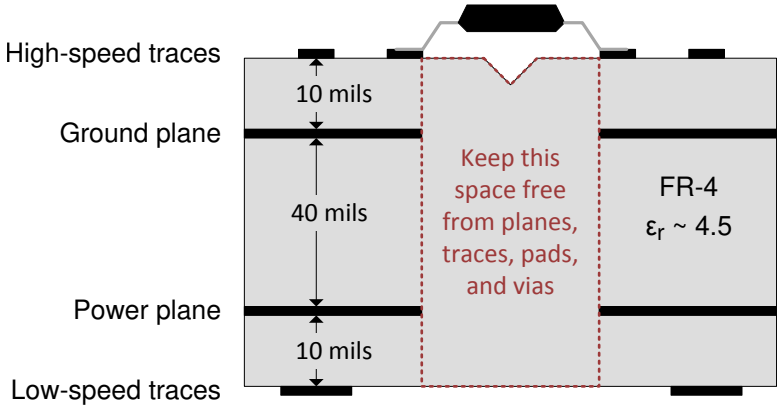


Figure 8-7. Layout Example Schematic

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators*, data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
ISO6163QDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	--40 to 125	ISO6163

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

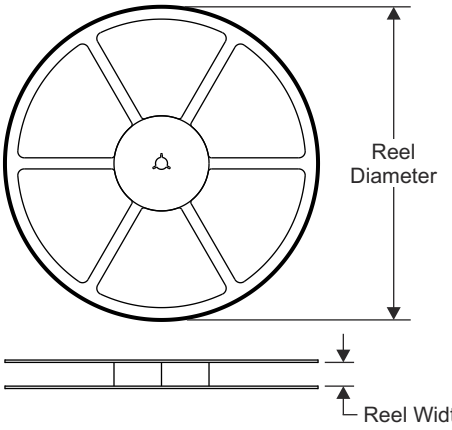
(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

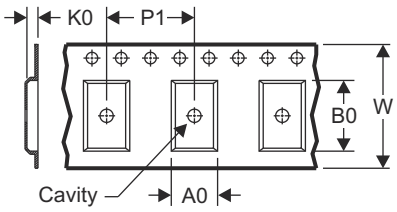
ADVANCE INFORMATION

11.2 Tape and Reel Information

REEL DIMENSIONS

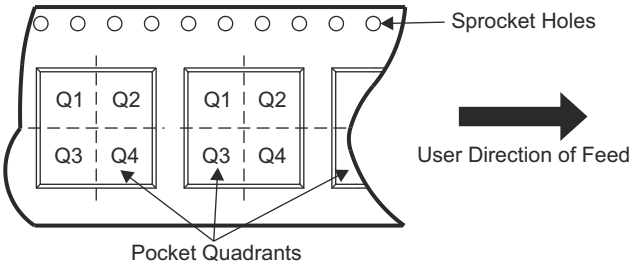


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

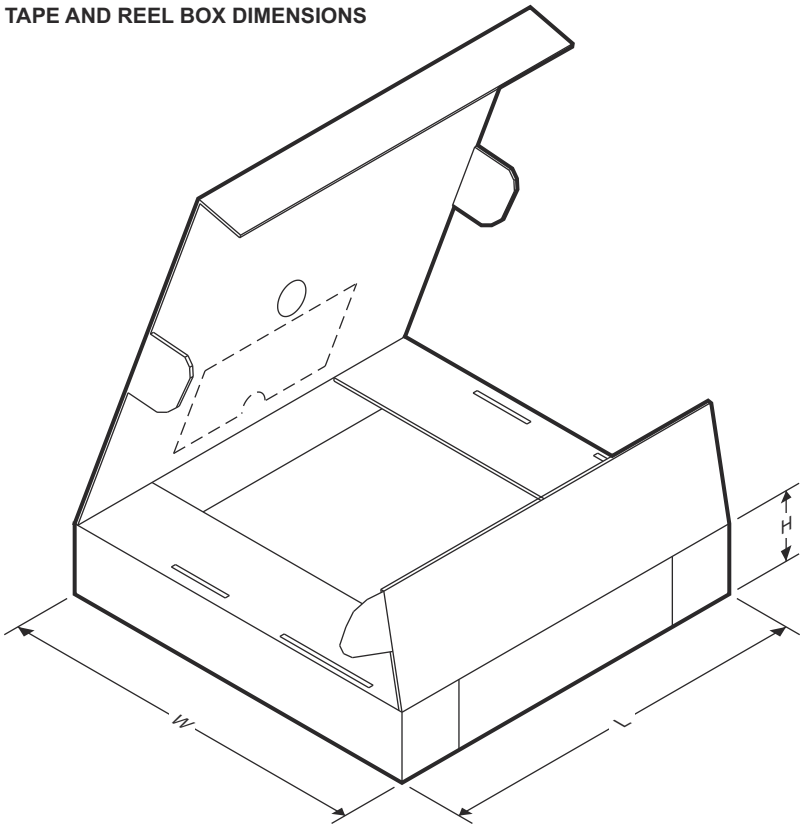


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6163QDWR	SOIC	DW	16	2000	330.0	24.4	10.9	10.7	2.7	12.0	24.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



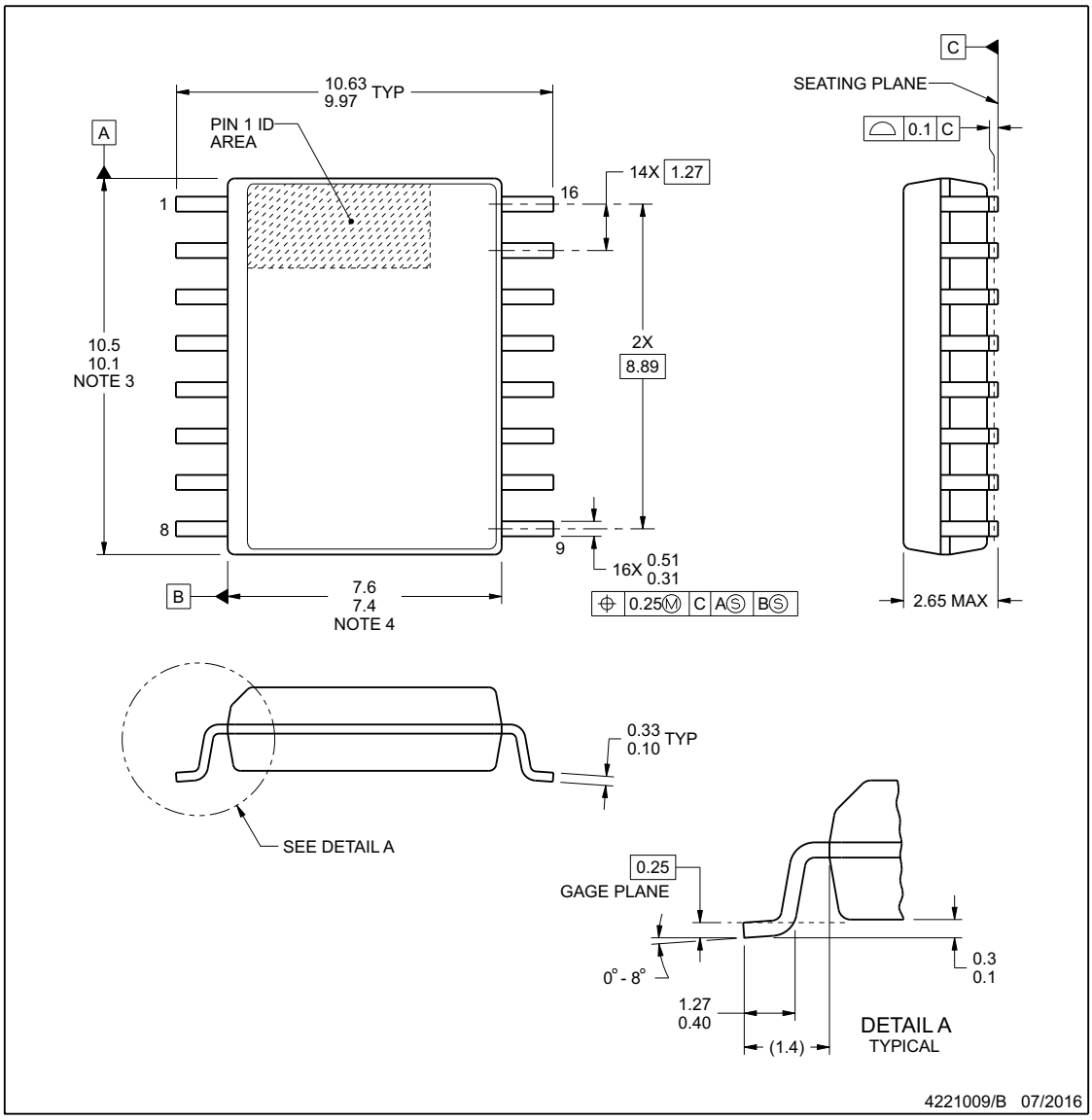
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6163QDWR	SOIC	DW	16	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

ADVANCE INFORMATION

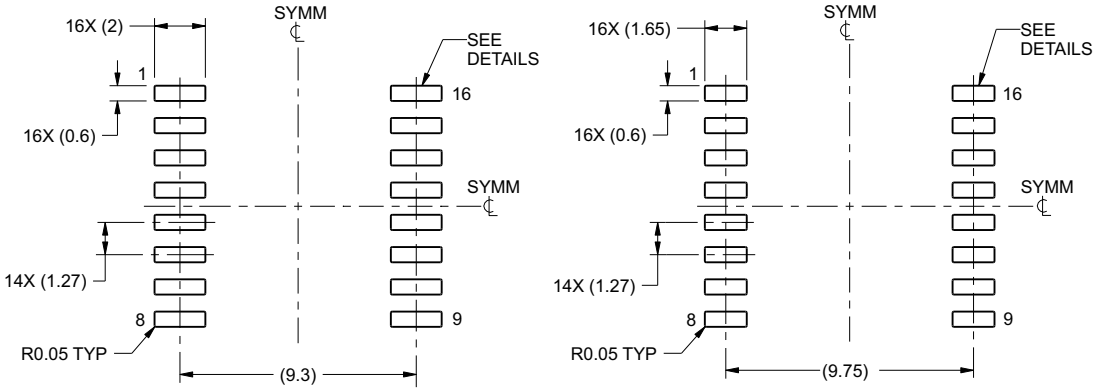
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

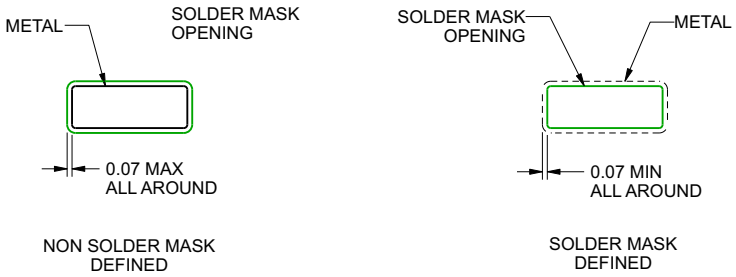
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

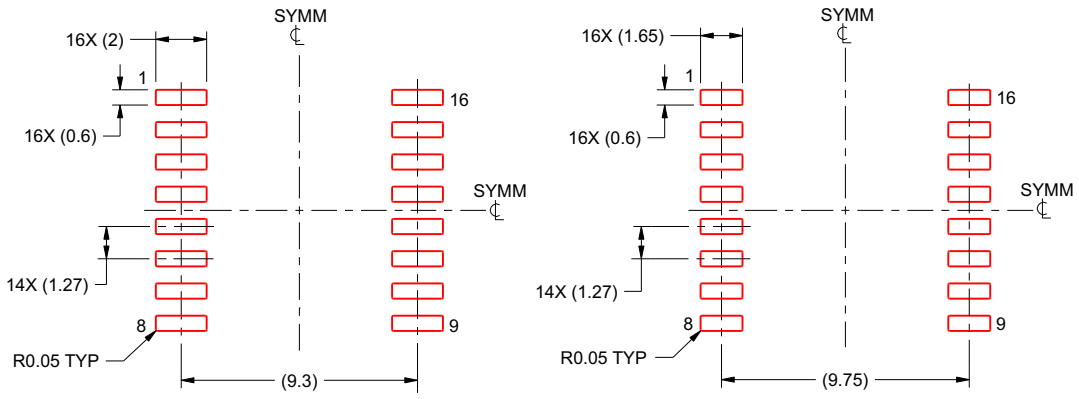
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

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