TMUXS7614D 50V, SPI Controlled, Low-RON, High Density, 1:1 (SPST), 8-Channel Precision Switches with 1.2V and 1.8V Logic

ADVANCE INFORMATION

1 Features

- Dual supply range: ±4.5V to ±25V
- Single supply range: 4.5V to 42V
- Asymmetric dual supply support (For example: V_{DD}=37.5V, V_{SS}=-12.5V)
- 1.2V and 1.8V logic compatible
- SPI supply range: 1.8V – 5.5V
- SPI Interface with support up to 50MHz
  - Manual mode (Standard SPI or Burst mode)
  - Daisy Chain mode
  - SPI error detection: CRC, invalid read/write, and clock count error
  - Industry standard modes 0 and 3
  - 1.8V logic compatible
- Ultra high channel density (2.5mm^2/ch)
  - Flow through SPI and supply routing for increased board density
  - Integrated decoupling capacitors
- Precision performance:
  - Low on-resistance: 1.1Ω (typical)
  - Ultra low on-resistance flatness: 0.003Ω (typical)
  - Low on-leakage current: 3.7pA (typical), 700pA (maximum)
  - Ultra low charge injection: 2pC (typical)
- High current support: 470mA per channel (maximum)
- –40°C to +125°C operating temperature
- Rail-to-rail operation
- Bidirectional operation
- Break-before-make switching

2 Applications

- Semiconductor test equipment
- SSR and photorelay replacement
- Automated test equipment
- LCD test equipment
- Memory test equipment
- Instrumentation: lab, analytical, and portable
- Data acquisition systems (DAQ)
- Optical test equipment

3 Description

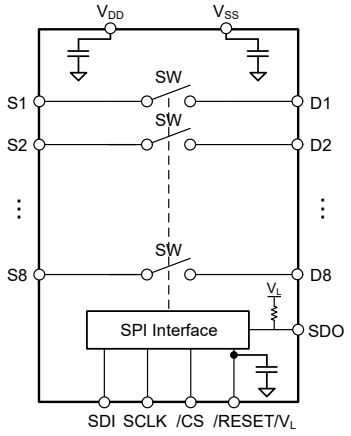
The TMUXS7614D is a complementary metal-oxide semiconductor (CMOS) switch device with eight independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works with a single supply (4.5V to 42V), dual supplies (±4.5V to ±25V), or asymmetric supplies (such as V_{DD} = 37.5V, V_{SS} = –12V). The TMUXS7614D supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.

The switches of the TMUXS7614D are controlled with a serial peripheral interface (SPI). The SPI interface has many error detection features, such as CRC, invalid read/write, and clock count error detection. The SPI also supports Daisy Chain mode. Coupled with the flow through routing of the SPI pins, this allows for increased channel density in the system. The TMUXS7614D is a part of the precision switches and multiplexers family of devices and have very low on and off leakage currents allowing them to be used in high precision measurement applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUXS7614D	ZEM (FCLGA, 30)	5mm × 4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUXS7614D Block Diagrams

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4 Pin Configuration and Functions

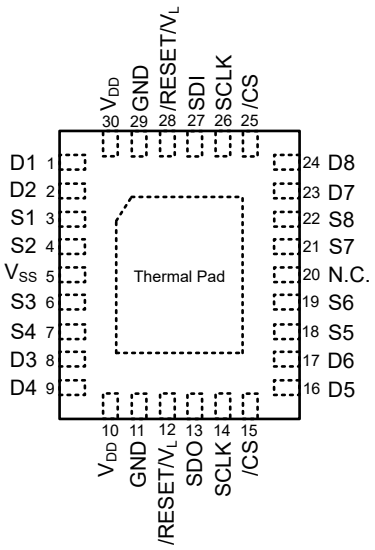

Figure 4-1. ZEM Package, 30-Pin LGA (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D1	1	I/O	Drain pin 1. Can be an input or output.
D2	2	I/O	Drain pin 2. Can be an input or output.
D3	8	I/O	Drain pin 3. Can be an input or output.
D4	9	I/O	Drain pin 4. Can be an input or output.
D5	16	I/O	Drain pin 5. Can be an input or output.
D6	17	I/O	Drain pin 6. Can be an input or output.
D7	23	I/O	Drain pin 7. Can be an input or output.
D8	24	I/O	Drain pin 8. Can be an input or output.
GND	11, 29	P	Ground (0V) reference. On TMUXS7614D, both GND pins are connected internally for flow through routing.
N.C.	20	O	No internal connection. Can be shorted to GND or left floating.
S1	3	I/O	Source pin 1. Can be an input or output.
S2	4	I/O	Source pin 2. Can be an input or output.
S3	6	I/O	Source pin 3. Can be an input or output.
S4	7	I/O	Source pin 4. Can be an input or output.
S5	18	I/O	Source pin 5. Can be an input or output.
S6	19	I/O	Source pin 6. Can be an input or output.
S7	21	I/O	Source pin 7. Can be an input or output.
S8	22	I/O	Source pin 8. Can be an input or output.
SDI	27	I	SPI Serial Data Input. Data is captured on the positive edge of SCLK.
SCLK	14, 26	I	SPI Clock Input. Both SCLK pins are connected internally for flow through routing.
SDO	13	O	SPI Serial Data Output. Data is shifted out on the negative edge of SCLK.
$\overline{CS}$	15, 25	I	SPI Chip Select Pin (active low). Both $\overline{CS}$ pins are connected internally for flow through routing.
$\overline{RESET}/V_L$	12, 28	P	SPI Power Supply pin (1.8V – 5.5V) and hardware reset pin (active low). Pull the pin low to trigger a device hardware reset. After the hardware reset is complete, the SPI registers will be reset to their default state, and all the analog switches will be open. Both $\overline{RESET}/V_L$ pins are connected internally for flow through routing. Connected to an integrated 0.1µF capacitor between V_L and GND.
VDD	10, 30	P	Positive power supply. This pin is the most positive power-supply potential. On TMUXS7614D, both VDD pins are connected internally for flow through routing. Connected to an integrated 0.1µF capacitor between V_{DD} and GND.
VSS	5	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin should be connected to ground. Connected to an integrated 0.1µF capacitor between V_{SS} and GND.
Thermal Pad		—	The thermal exposed pad is connected internally. It is recommended that the pad be tied to VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		50	V
V_{DD}		–0.5	50	V
V_{SS}		–32	0.5	V
V_L	Logic Supply Voltage	–0.5	6	V
V_{LOGIC}	Logic control input pin voltage (SPI pins)	–0.5	6	V
I_{LOGIC}	Logic control input pin current (SPI pins)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation		1650	mW

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,
functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	TBD	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC (1)		TMUXS7614D ZEM (LGA) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.30	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	41.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	4.5		50	V
V_{DD}	Positive power supply voltage	4.5		42	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_L	Logic Supply Voltage	1.8		5.5	V
V_{LOGIC}	Logic control input pin voltage (SPI pins)	0		5.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (2)	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Current through Switch

Current through the Switch	Test Conditions	T_J = 25°C	T_J = 50°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	T_J = 135°C	T_J = 150°C	UNIT
I_{DC} (1)	V_{SS} to V_{DD} - 2.5V	470	470	470	309	143	100	60	mA
I_{peak} (2)	V_{SS} to V_{DD} - 2.5V	470	470	470	470	470	470	470	mA

(1) See ***Thermal Considerations*** section for more details
(2) Pulse current of 1ms with 10% Duty Cycle

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5.6 Electrical Characteristics (Global)

Over operating supply voltage range, V_L = 1.8V - 5.5V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, V_L = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SPI pins)							
V_{IH}	Logic voltage high	V_L = 5.5 V	–40°C to +125°C	2			V
		V_L = 3.3 V	–40°C to +125°C	1.35			V
		V_L < 1.8 V	–40°C to +125°C	1			V
V_{IL}	Logic voltage low	2.7 V ≤ V_L ≤ 5.5 V	–40°C to +125°C			0.75	V
		1.8 V ≤ V_L < 2.7 V	–40°C to +125°C			0.5	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–2	–0.005		µA
T_{SD}	Thermal shutdown				165		°C
T_{SD_HYST}	Thermal shutdown hysteresis				15		°C
V_{OH}	Logic high output voltage	I_{SOURCE} = 100 µA	–40°C to +125°C	V_L - 0.1			V
		I_{SOURCE} = 1 mA	–40°C to +125°C	V_L - 0.7			V
V_{OL}	Logic low output voltage	I_{SINK} = 100 µA	–40°C to +125°C			0.1	V
		I_{SINK} = 1 mA	–40°C to +125°C			0.7	V
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{LQ}	V_L quiscent supply current	V_L = 1.8 V to 5.5 V SPI Inputs = 0 V or V_L	25°C		5	6	µA
			–40°C to +85°C			7	µA
			–40°C to +125°C			8	µA
I_L	V_L active supply current	V_L = 2.7 V to 5.5 V /CS = 0V, fSCLK = 50 MHz, fSDI = 25 MHz	25°C		1	1.2	mA
			–40°C to +85°C			1.5	mA
			–40°C to +125°C			2	mA

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5.7 Electrical Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10% GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		1.1	1.4	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.8	
			–40°C to +125°C			2.2	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.03	
			–40°C to +85°C			0.035	
			–40°C to +125°C			0.038	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.003		Ω
			–40°C to +50°C			0.035	
			–40°C to +85°C			0.035	
			–40°C to +125°C			0.035	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.03	0.15	nA
			–40°C to +50°C	–0.3		0.3	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–12		12	
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.03	0.15	nA
			–40°C to +50°C	–0.3		0.3	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–12		12	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–0.6	0.013	0.6	nA
			–40°C to +50°C	-0.75		0.75	
			–40°C to +85°C	–0.8		0.8	
			–40°C to +125°C	–9		9	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C		4		pA
			–40°C to +50°C		4.5		
			–40°C to +85°C		6		
			–40°C to +125°C		27		
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		45	80	µA
			–40°C to +85°C			90	
			–40°C to +125°C			115	
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		840	1110	µA
			–40°C to +85°C			1120	
			–40°C to +125°C			1125	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		15	30	µA
			–40°C to +85°C			45	
			–40°C to +125°C			65	

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5.7 Electrical Characteristics (±15 V Dual Supply) (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10% GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		680	800	µA
			–40°C to +85°C			850	
			–40°C to +125°C			900	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

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5.8 Switching Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.0	2.5	µs
			–40°C to +85°C			2.75	µs
			–40°C to +125°C			3	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		310		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–74		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		180		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–80		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0001		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		27		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		27		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		22		pF

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5.9 Electrical Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		1.1	1.4	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.9	
			–40°C to +125°C			2.2	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.004		Ω
			–40°C to +50°C			0.038	
			–40°C to +85°C			0.048	
			–40°C to +125°C			0.048	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.006		Ω
			–40°C to +50°C			0.04	
			–40°C to +85°C			0.04	
			–40°C to +125°C			0.04	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.005		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.16	0.012	0.16	nA
			–40°C to +50°C	-0.425		0.425	
			–40°C to +85°C	–3.4		3.4	
			–40°C to +125°C	–31		31	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.16	0.012	0.16	nA
			–40°C to +50°C	-0.425		0.425	
			–40°C to +85°C	–3.4		3.4	
			–40°C to +125°C	–31		31	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–0.8	0.0045	0.8	nA
			–40°C to +50°C	-1		1	
			–40°C to +85°C	–1.3		1.3	
			–40°C to +125°C	–6.5		6.5	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		45	80	µA
			–40°C to +85°C			90	
			–40°C to +125°C			115	
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		840	1110	µA
			–40°C to +85°C			1120	
			–40°C to +125°C			1125	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		15	30	µA
			–40°C to +85°C			45	
			–40°C to +125°C			65	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		680	800	µA
			–40°C to +85°C			850	
			–40°C to +125°C			900	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.10 Switching Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2	2.5	µs
			–40°C to +85°C			2.9	µs
			–40°C to +125°C			3	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.8	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			2.8	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	150			ns
			–40°C to +125°C	150			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–76		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V,	25°C		200		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.093		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–76		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0001		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		24		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		24		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		21		pF

ADVANCE INFORMATION

5.11 Electrical Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		1.1	1.35	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.8	
			–40°C to +125°C			2.1	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.04	
			–40°C to +85°C			0.04	
			–40°C to +125°C			0.04	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.006		Ω
			–40°C to +50°C			0.05	
			–40°C to +85°C			0.05	
			–40°C to +125°C			0.05	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.3	0.021	0.3	nA
			–40°C to +50°C	–0.75		0.75	
			–40°C to +85°C	–5.5		5.5	
			–40°C to +125°C	–45		45	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.3	0.021	0.3	nA
			–40°C to +50°C	–0.75		0.75	
			–40°C to +85°C	–5.5		5.5	
			–40°C to +125°C	–45		45	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is on V_S = V_D = 32.5 V or –7.5 V	25°C	-0.85	0.02	0.85	nA
			–40°C to +50°C	-1.05		1.05	
			–40°C to +85°C	–1.3		1.3	
			–40°C to +125°C	–10		10	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is on V_S = V_D = 32.5 V or –7.5 V	25°C		1.1		pA
			–40°C to +50°C		2.1		
			–40°C to +85°C		4		
			–40°C to +125°C		12.1		
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		45	80	µA
			–40°C to +85°C			95	
			–40°C to +125°C			120	
I_{DD}	V_{DD} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		840	1110	µA
			–40°C to +85°C			1120	
			–40°C to +125°C			1125	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		17	30	µA
			–40°C to +85°C			45	
			–40°C to +125°C			65	

ADVANCE INFORMATION

5.11 Electrical Characteristics (+37.5 V/–12.5 V Dual Supply) (continued)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{SS}	V_{SS} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		680	800	µA
			–40°C to +85°C			850	
			–40°C to +125°C			900	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

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5.12 Switching Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V ±10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.1	3	µs
			–40°C to +85°C			3.5	µs
			–40°C to +125°C			4	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.74	2	µs
			–40°C to +85°C			2.1	µs
			–40°C to +125°C			2.5	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		350		ns
			–40°C to +85°C	310			ns
			–40°C to +125°C	300			ns
Q_{INJ}	Charge injection	V_S = 12.5 V, C_L = 100 pF	25°C		6.5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–75		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V,	25°C		200		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–0.093		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–80		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		24		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		24		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		21		pF

ADVANCE INFORMATION

5.13 Electrical Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 3 V to 9 V I_D = –10 mA	25°C		1.15	1.6	Ω
			–40°C to +50°C			1.75	
			–40°C to +85°C			2	
			–40°C to +125°C			2.3	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.05	
			–40°C to +85°C			0.05	
			–40°C to +125°C			0.05	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.084		Ω
			–40°C to +50°C			0.13	
			–40°C to +85°C			0.14	
			–40°C to +125°C			0.16	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.07	0.0035	0.07	nA
			–40°C to +50°C	–0.16		0.16	
			–40°C to +85°C	–0.6		0.6	
			–40°C to +125°C	–12		12	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.07	0.0027	0.07	nA
			–40°C to +50°C	–0.16		0.16	
			–40°C to +85°C	–0.6		0.6	
			–40°C to +125°C	–12		12	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 1 V or 10 V	25°C	–0.7	0.003	0.7	nA
			–40°C to +50°C	-0.85		0.85	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–8		8	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 13.2 V, V_{SS} = 0 V All switches OFF	25°C		30	65	µA
			–40°C to +85°C			100	
			–40°C to +125°C			115	
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V All switches ON	25°C		840	1110	µA
			–40°C to +85°C			1120	
			–40°C to +125°C			1125	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

ADVANCE INFORMATION

5.14 Switching Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		2	2.5	µs
			–40°C to +85°C			3	µs
			–40°C to +125°C			3.5	µs
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	160			ns
			–40°C to +125°C	160			ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–70		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V	25°C		165		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–78		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0095		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		37		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		37		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		27		pF

5.15 SPI Timing Characteristics (2.7 V to 5.5 V)

V_{LL} = 2.7V - 5.5V, GND = 0 V (unless otherwise noted)
Typical at V_{LL} = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{CLK_SPI}	SCLK Frequency		–40°C to +125°C			50	MHz
t_R, t_{F_SPI}	SPI Clock Rise and Fall Times		–40°C to +125°C			50	ns
t_{CLK_SPI}	SCLK Period		–40°C to +125°C	20			ns
$t_{CLK\_H\_SPI}$	SCLK High Time		–40°C to +125°C	8			ns
$t_{CLK\_L\_SPI}$	SCLK Low Time		–40°C to +125°C	8			ns

5.15 SPI Timing Characteristics (2.7 V to 5.5 V) (continued)

V_{LL} = 2.7V - 5.5V, GND = 0 V (unless otherwise noted)
Typical at V_{LL} = 3.3V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK		–40°C to +125°C	10			ns
t_{SU_SPI}	Set Up Time SDI to SCLK		–40°C to +125°C	6			ns
t_{H_SPI}	Hold Time SDI to SCLK		–40°C to +125°C	8			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$		–40°C to +125°C	10			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20 pF	–40°C to +125°C			25	ns
t_{SDO}	SCLK falling edge to SDO	20 pF	–40°C to +125°C			25	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20 pF	–40°C to +125°C			25	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands		–40°C to +125°C	20			ns
$t_{CSLSCLK}$	CS falling edge to SCLK becomes stable		–40°C to +125°C	8			ns
$t_{CSHSCLK}$	CS rising edge to SCLK becomes stable		–40°C to +125°C	8			ns

5.16 SPI Timing Characteristics (1.8 V to 2.7 V)

V_{LL} = 1.8V - 2.7V, GND = 0 V (unless otherwise noted)
Typical at V_{LL} = 1.8V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{CLK_SPI}	SCLK Frequency		–40°C to +125°C			25	MHz
t_R, t_{F_SPI}	SPI Clock Rise and Fall Times		–40°C to +125°C			25	ns
t_{CLK_SPI}	SCLK Period		–40°C to +125°C	40			ns
$t_{CLK\_H\_SPI}$	SCLK High Time		–40°C to +125°C	16			ns
$t_{CLK\_L\_SPI}$	SCLK Low Time		–40°C to +125°C	16			ns
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK		–40°C to +125°C	20			ns
t_{SU_SPI}	Set Up Time SDI to SCLK		–40°C to +125°C	12			ns
t_{H_SPI}	Hold Time SDI to SCLK		–40°C to +125°C	18			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$		–40°C to +125°C	20			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20 pF	–40°C to +125°C			50	ns
t_{SDO}	SCLK falling edge to SDO	20 pF	–40°C to +125°C			50	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20 pF	–40°C to +125°C			50	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands		–40°C to +125°C	40			ns
$t_{CSLSCLK}$	CS falling edge to SCLK becomes stable		–40°C to +125°C	16			ns
$t_{CSHSCLK}$	CS rising edge to SCLK becomes stable		–40°C to +125°C	16			ns

ADVANCE INFORMATION

5.17 Timing Diagrams

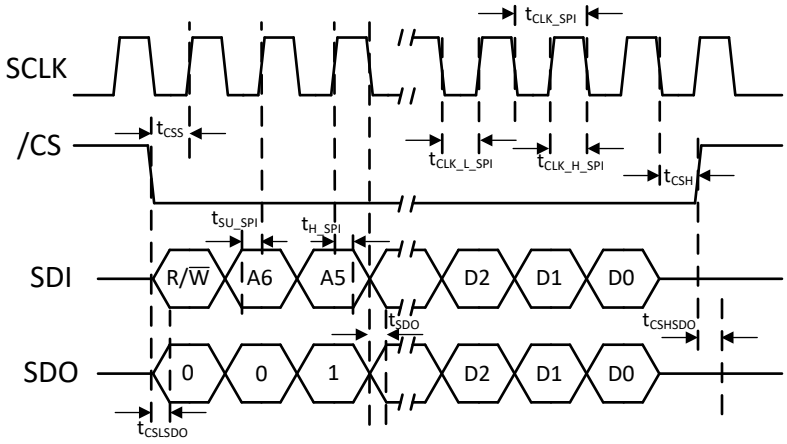

Figure 5-1. SPI Timing Diagram

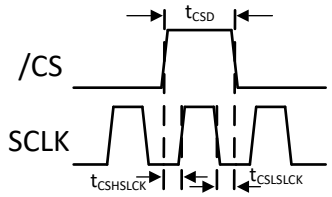

Figure 5-2. SCLK and /CS Timing Relationship

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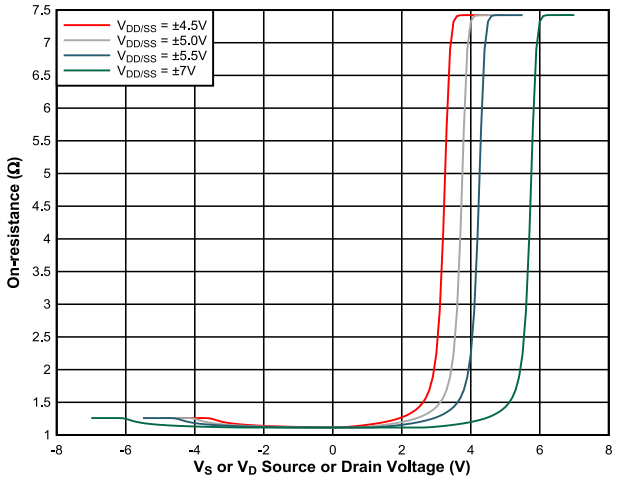
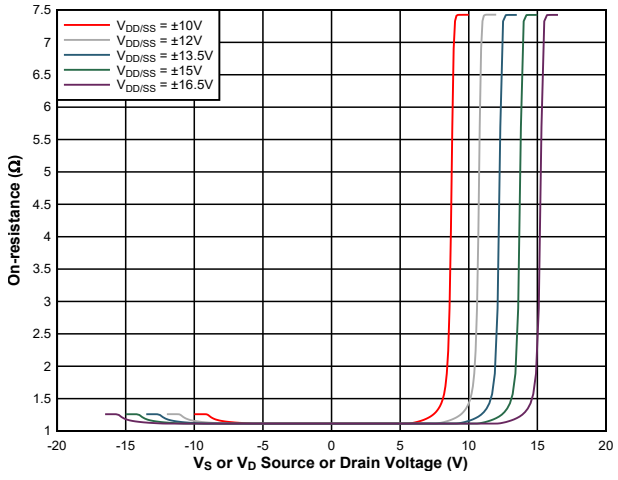
5.18 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



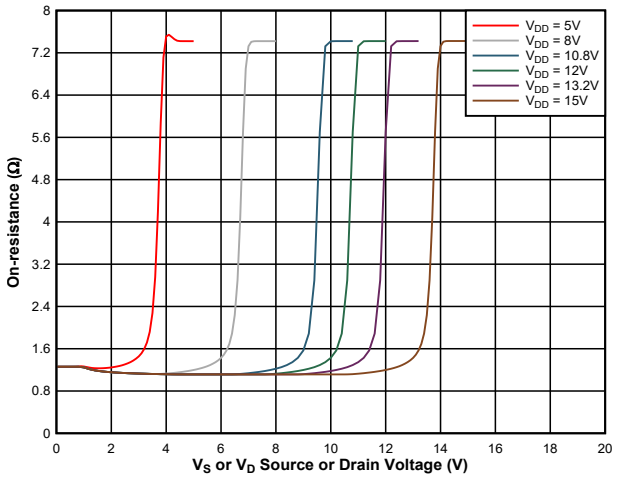
T_A = 25°

Figure 5-3. On-Resistance vs Source or Drain Voltage



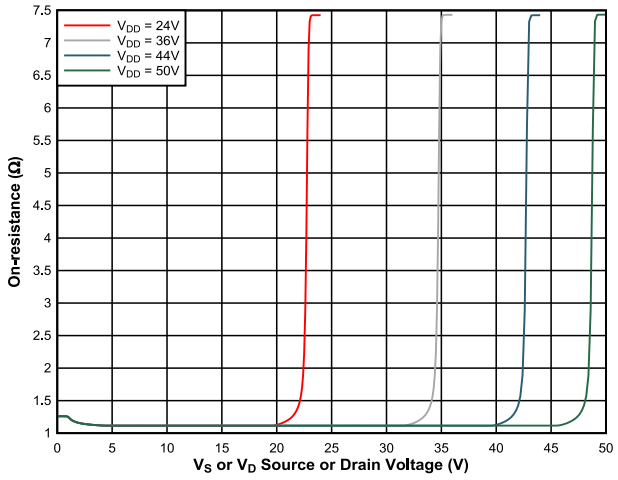
T_A = 25°

Figure 5-4. On-Resistance vs Source or Drain Voltage



T_A = 25°

Figure 5-5. On-Resistance vs Source or Drain Voltage



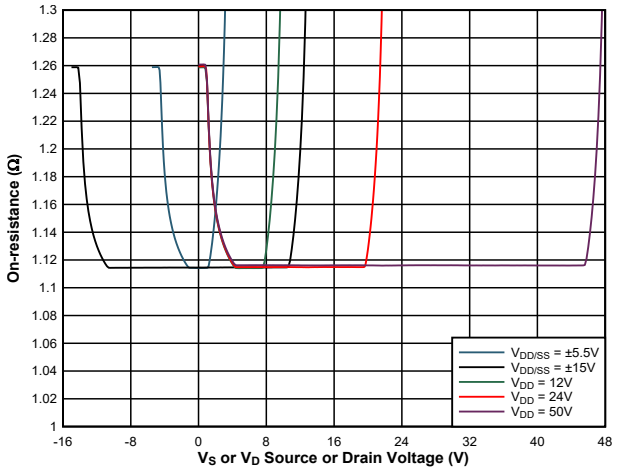
T_A = 25°

Figure 5-6. On-Resistance vs Source or Drain Voltage

ADVANCE INFORMATION

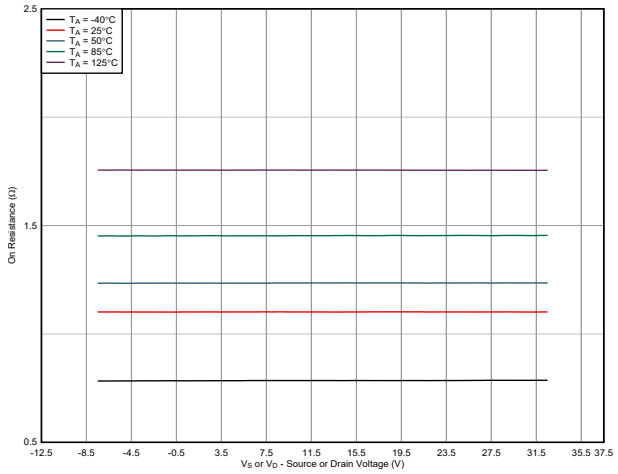
5.18 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



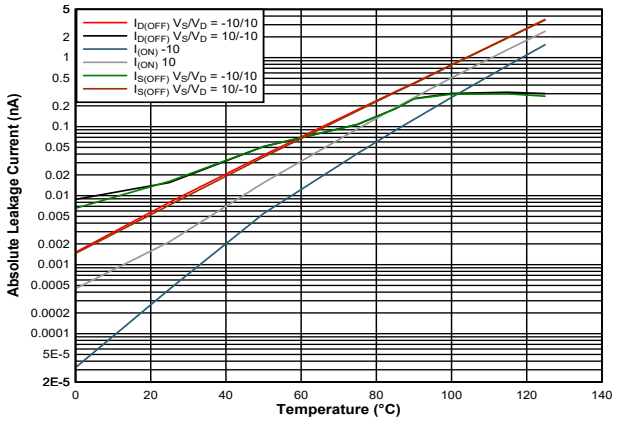
T_A = 25°

Figure 5-7. On-Resistance vs Source or Drain Voltage



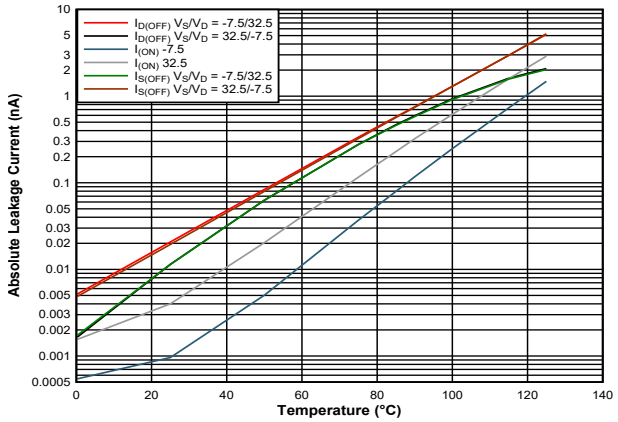
V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-8. On-Resistance vs Source or Drain Voltage



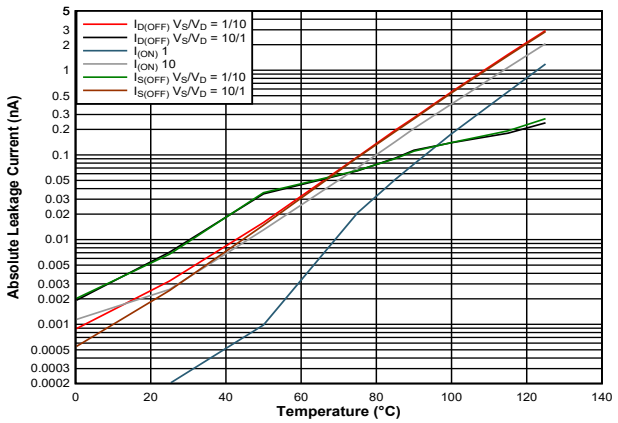
V_{DD} = 15V, V_{SS} = -15V

Figure 5-9. Leakage Current vs Temperature



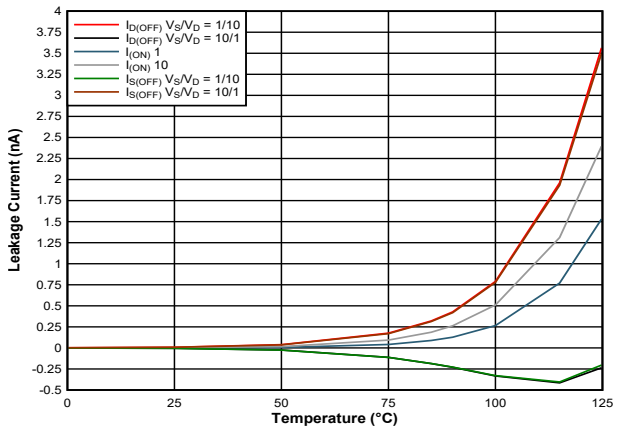
V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-10. Leakage Current vs Temperature



V_{DD} = 12V, V_{SS} = 0V

Figure 5-11. Leakage Current vs Temperature

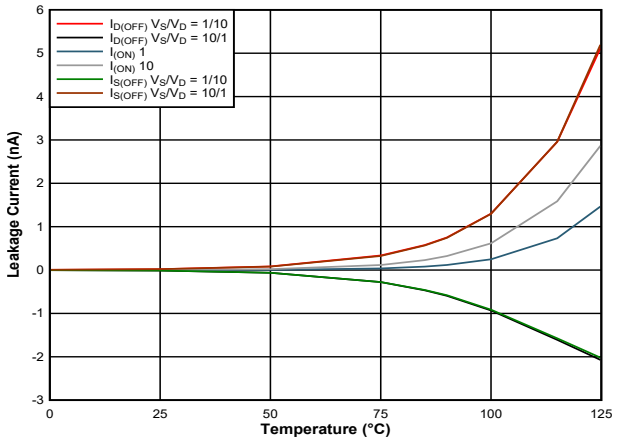


V_{DD} = 15V, V_{SS} = -15V

Figure 5-12. Leakage Current vs Temperature

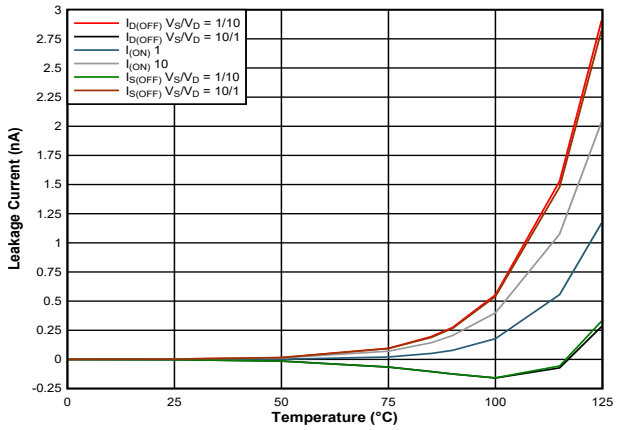
5.18 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



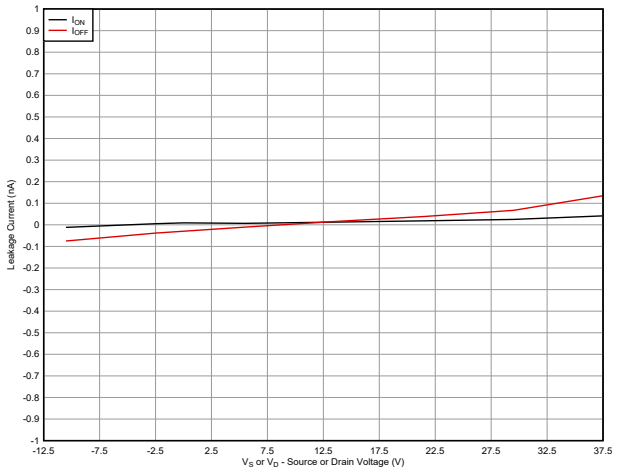
V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-13. Leakage Current vs Temperature



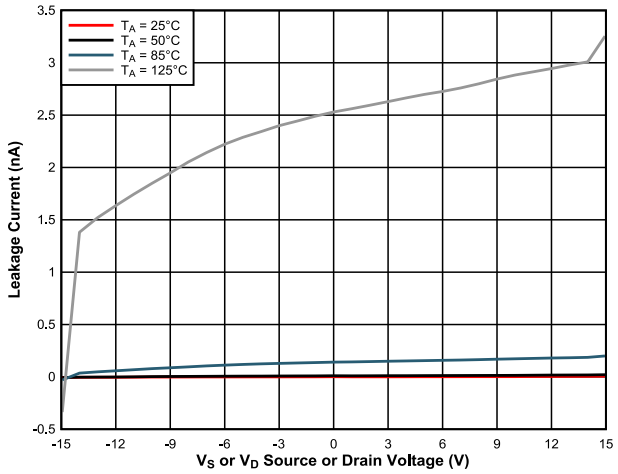
bV_{DD} = 12V, V_{SS} = 0V

Figure 5-14. Leakage Current vs Temperature



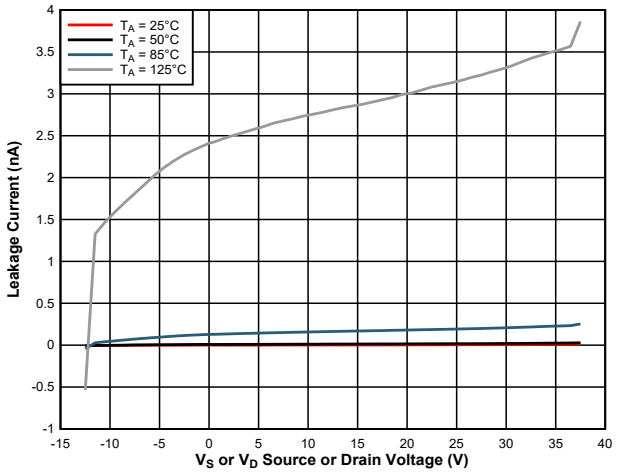
V_{DD} = 37.5V, V_{SS} = -12.5V, T_A = 50°C

Figure 5-15. On Leakage Current vs Source or Drain Voltage



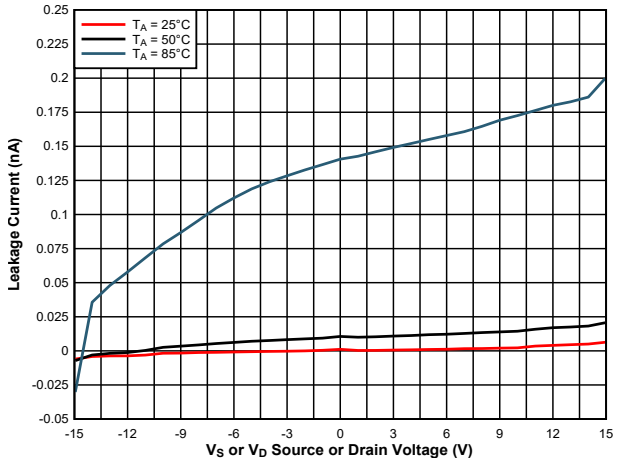
V_{DD} = 15V, V_{SS} = -15V

Figure 5-16. On Leakage Current vs Source or Drain Voltage



V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-17. On Leakage Current vs Source or Drain Voltage



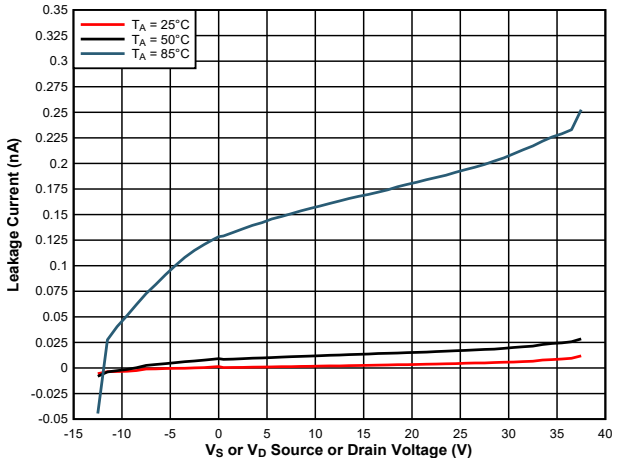
V_{DD} = 15V, V_{SS} = -15V

Figure 5-18. On Leakage Current vs Source or Drain Voltage

ADVANCE INFORMATION

5.18 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-19. On Leakage Current vs Source or Drain Voltage

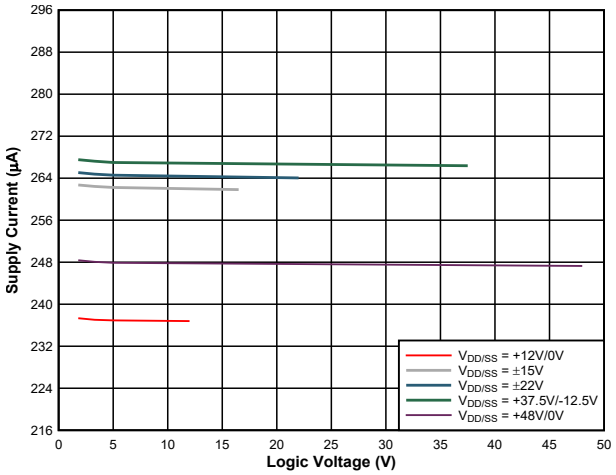


Figure 5-20. Supply Current vs Logic Voltage

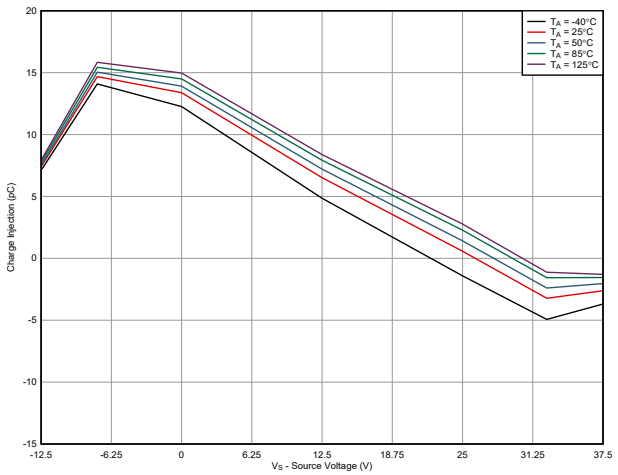


Figure 5-21. Charge Injection vs Source Voltage

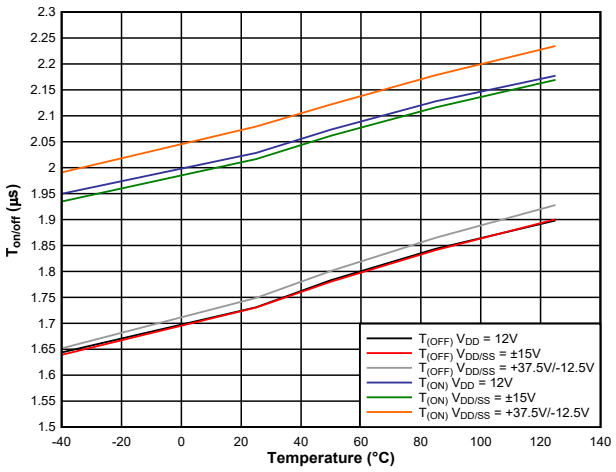


Figure 5-22. Turn on/off time vs Temperature

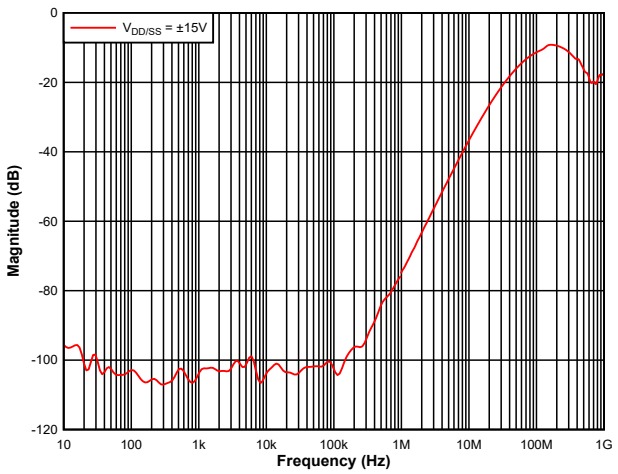


Figure 5-23. Off-Isolation vs Frequency

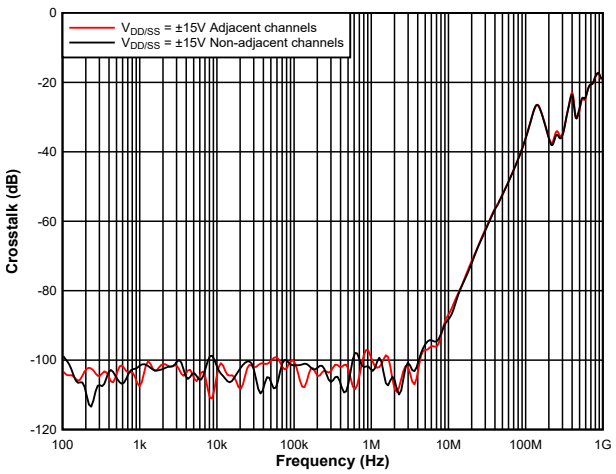


Figure 5-24. Crosstalk vs Frequency

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5.18 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

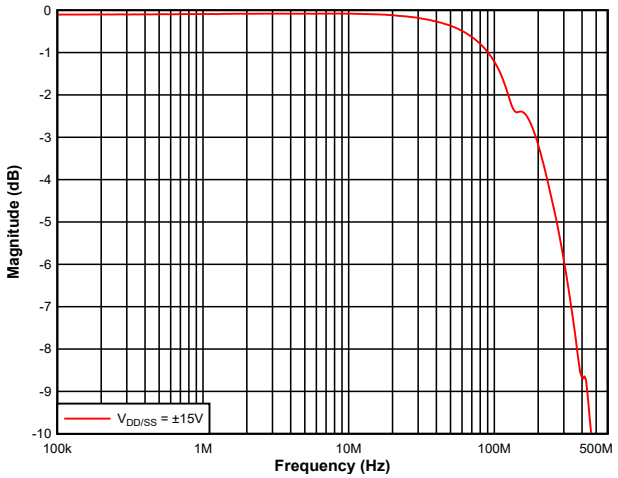

Figure 5-25. Bandwidth vs Frequency

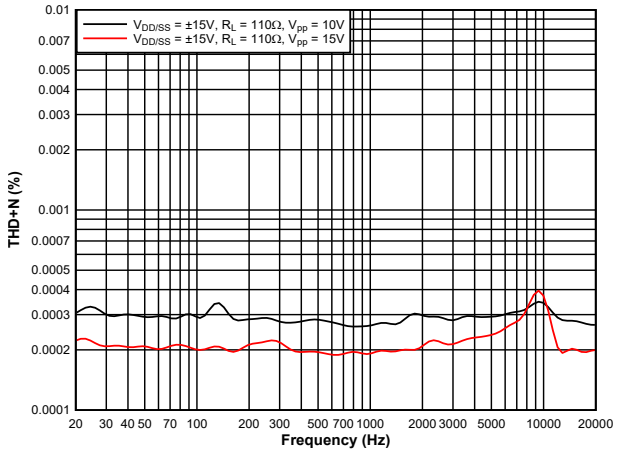

Figure 5-26. THD+N vs Frequency

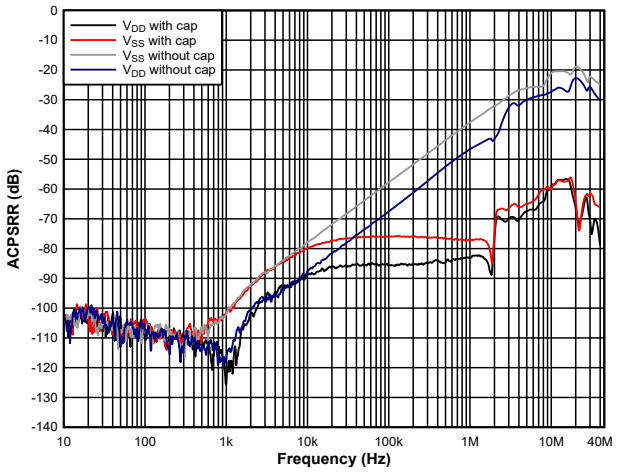

Figure 5-27. ACPSRR vs Frequency

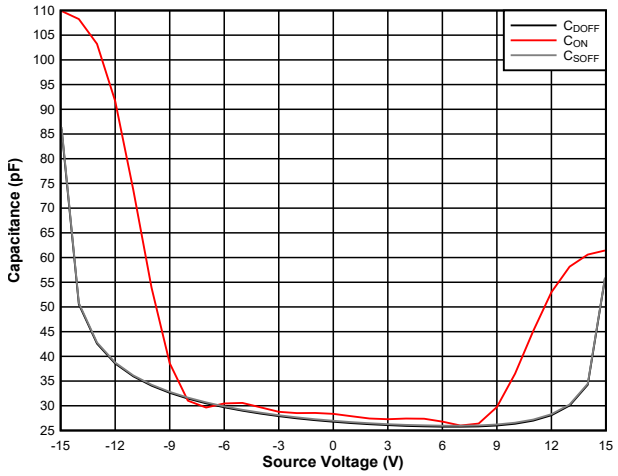

Figure 5-28. Capacitance vs Source or Drain Voltage

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6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

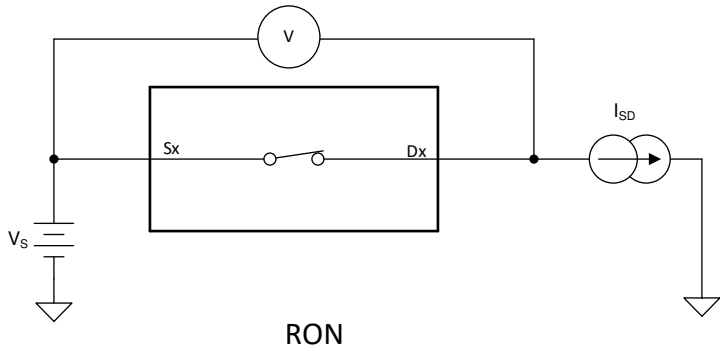

Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

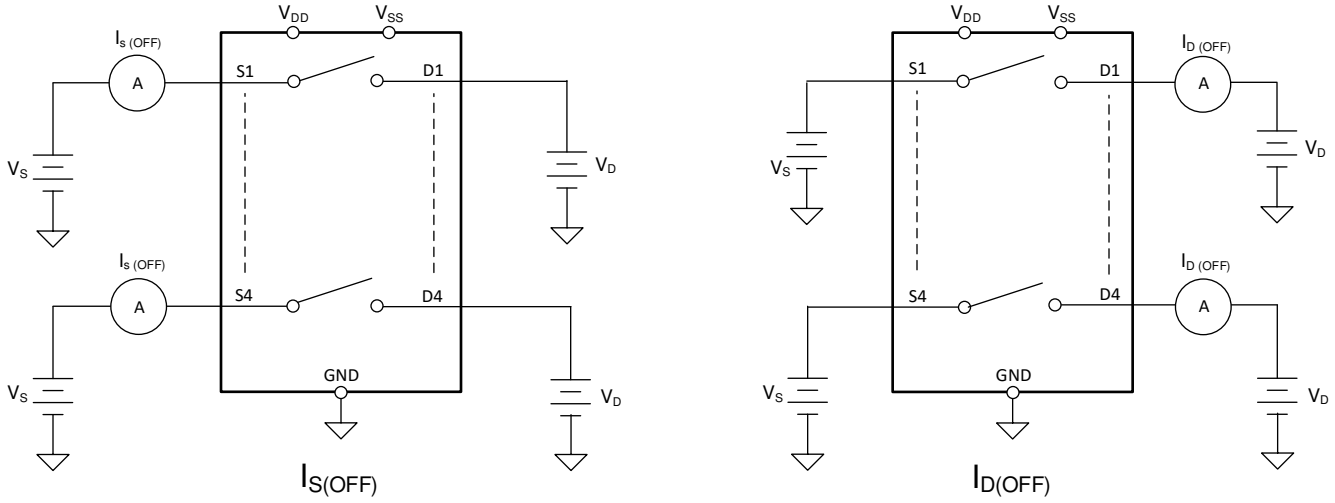

Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

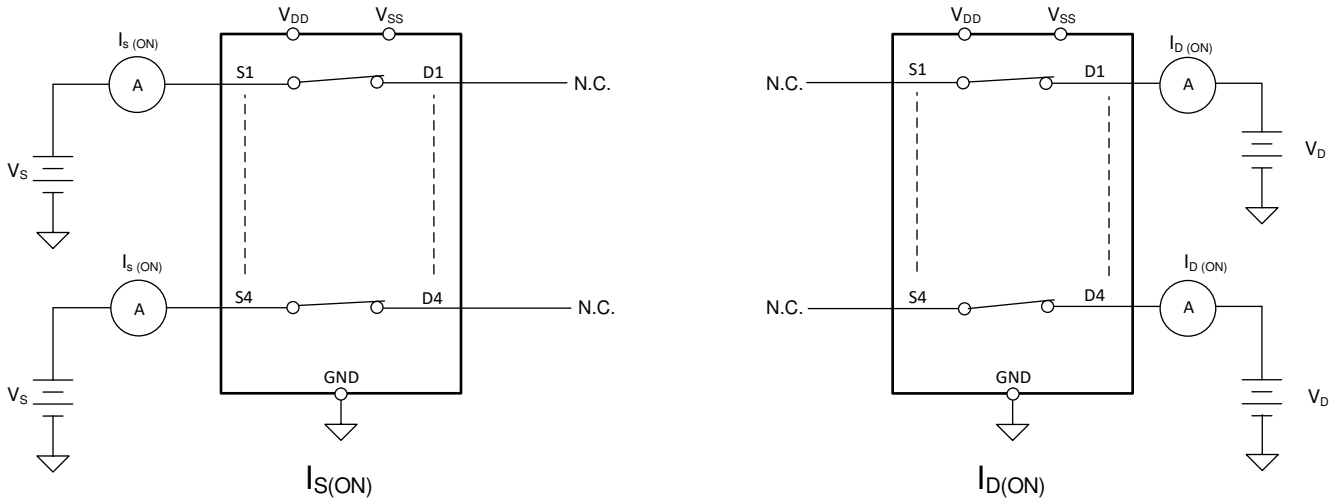

Figure 6-3. On-Leakage Measurement Setup

6.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

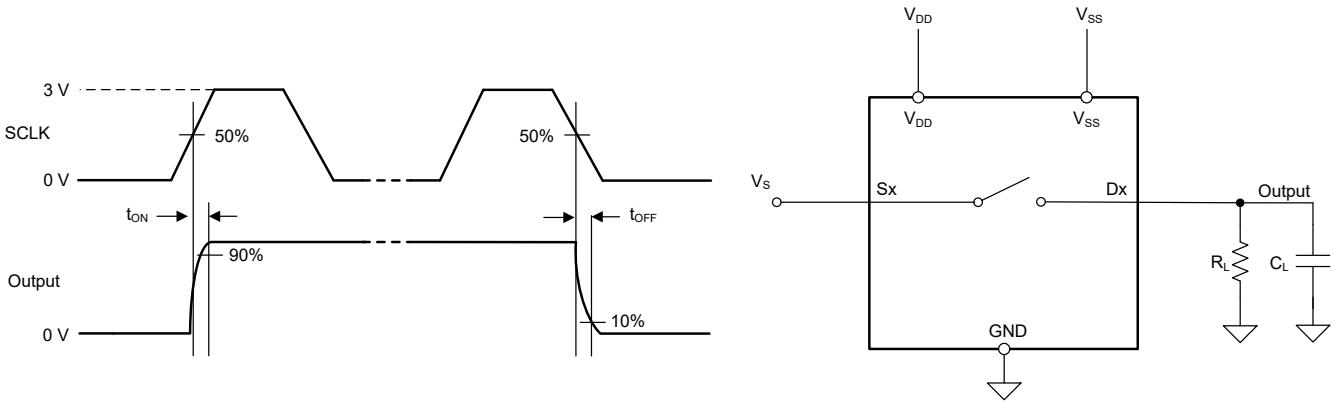

Figure 6-4. Turn-On and Turn-Off Time Measurement Setup

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6.5 Break-Before-Make

The TMUXS7614D has break-before-make delay which allows the device to be used in cross-point switching application. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

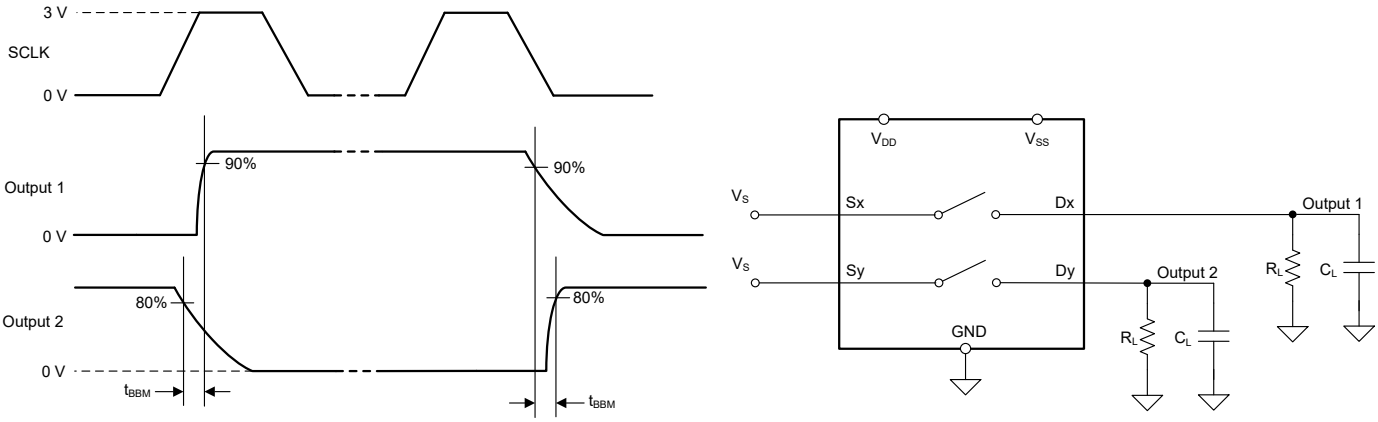


Figure 6-5. Break-Before-Make Delay Measurement Setup

6.6 Charge Injection

The TMUXS7614D devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

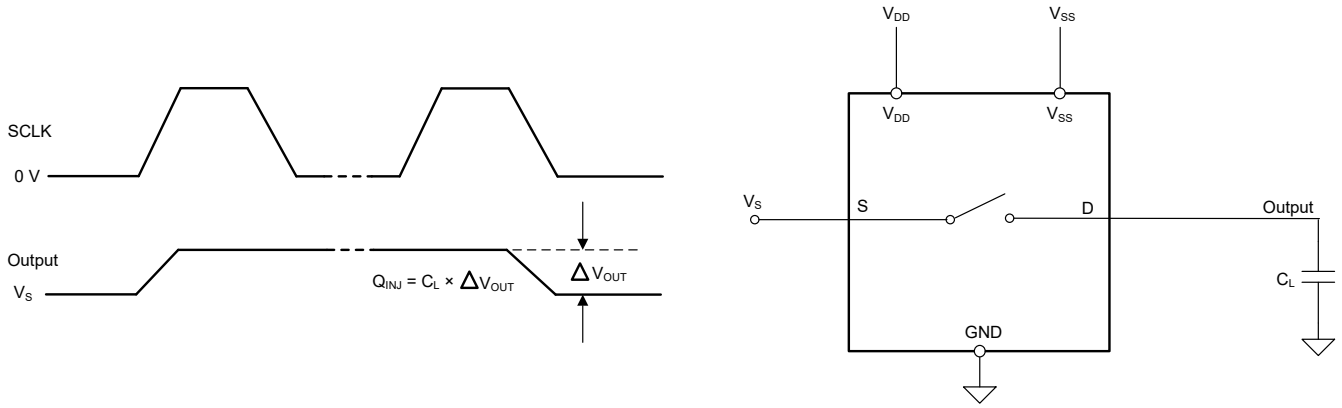
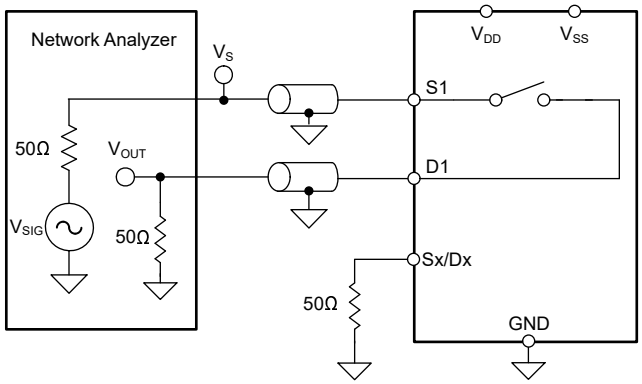


Figure 6-6. Charge-Injection Measurement Setup

6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-7 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

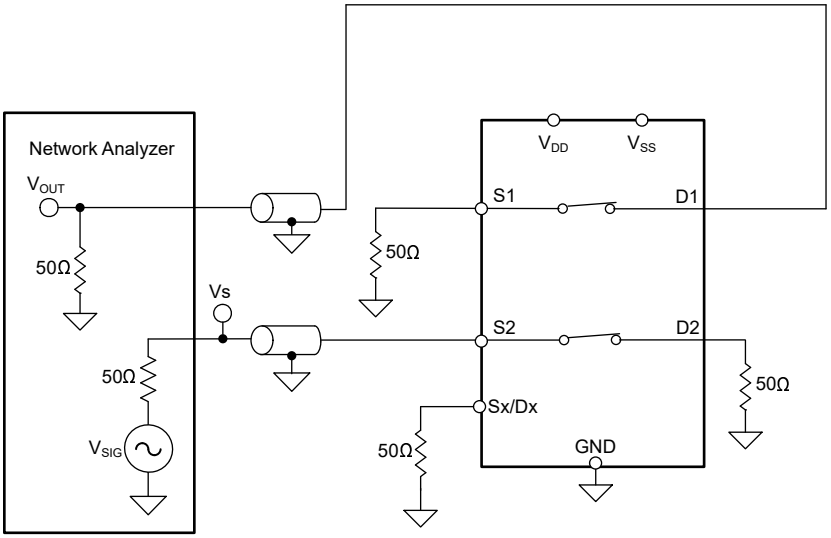


$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

Figure 6-7. Off Isolation Measurement Setup

6.8 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-8 shows the setup used to measure, and the equation used to compute crosstalk.



$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

Figure 6-8. Channel-to-Channel Crosstalk Measurement Setup

6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-9 shows the setup used to measure bandwidth.

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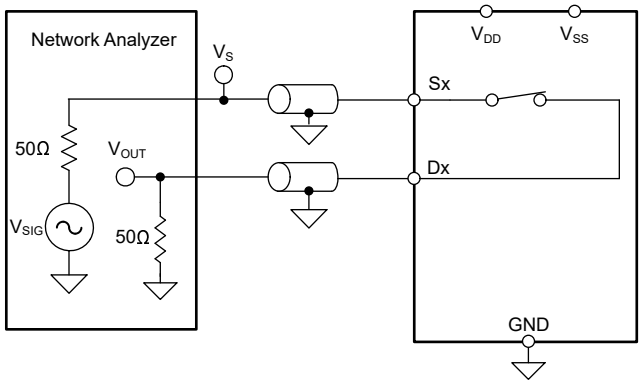


Figure 6-9. Bandwidth Measurement Setup

$$\text{Bandwidth} = 20 \times \text{Log}\left(\frac{\text{Vout}}{\text{Vs}}\right) \quad (1)$$

6.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

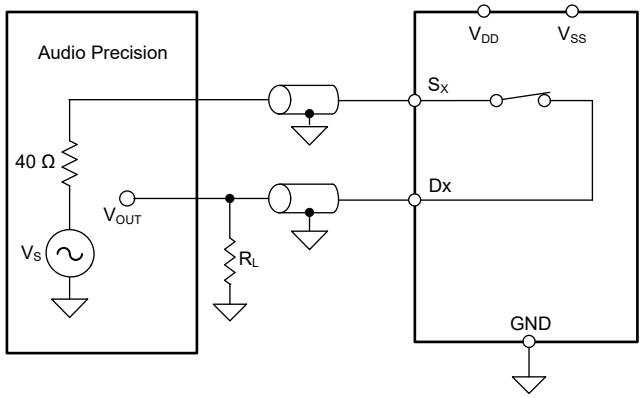


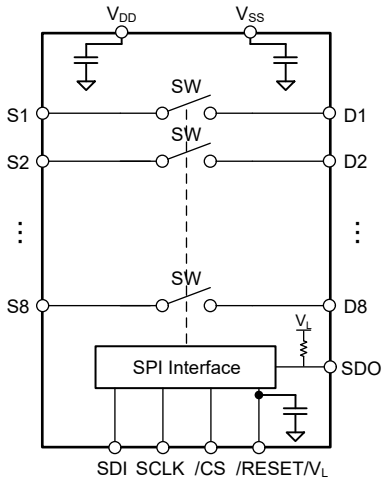
Figure 6-10. THD + N Measurement Setup

7 Detailed Description

7.1 Overview

The TMUXS7614D is a 1:1 (SPST), 8-channel switch. This device has eight independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the SPI registers. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 37.5V, V_{SS} = –12V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUXS7614D conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUXS7614D ranges from V_{SS} to V_{DD}.

7.3.3 1.8V Logic Compatible Inputs

The TMUXS7614D has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUXS7614D to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. Additionally, VL supports 1.8V – 5.5V, and SDO is based on VL. So no additional translator is needed to support SPI readback. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

7.3.4 Flat On-Resistance

The TMUXS7614D is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in precision applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

This architecture also ensures that RON stays the same regardless of the supply voltage. The flattest on-resistance region extends from VSS to roughly 5V below VDD. The on-resistance will exponentially increase when the signal is within 5V of VDD, which may impact the desired signal transmission.

7.3.5 Power-Up Sequence Free

The TMUXS7614D supports any power up sequencing. With the three supply rails (VDD, VSS, and VL), any rail can be powered on first. Similarly when powering down, the supply rails can be powered down in any order.

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7.4 SPI Operation

TMUXS7614D is SPI controlled with eight SPST switches and has SPI error detection features. SPI data input on SDI is sampled on the positive edge of SCLK, but SPI output data on SDO gets shifted out on the negative edge of SCLK. TMUXS7614D is compatible with SPI modes 0 and 3. While in the default mode, address mode, TMUXS7614D registers are accessed with 16-bit SPI commands sent while $\overline{CS}$ is pulled low. Burst Mode and Daisy Chain Mode are other modes that TMUXS7614D can operate within. The following is a list of error detection features offered:

1. Address R/W Error Flag
2. SCLK Count Error Flag
3. CRC (Cyclic Redundancy Check) Enable and Error Flag
4. Clearing Error Flags

TMUXS7614D SPI pins include SDI, SDO, SCLK and $\overline{CS}$.

7.4.1 Address Mode

The default state of TMUXS7614D is address mode. While in address mode the SPI frame expects the following sequence:

1. $\overline{CS}$ is pulled low
2. Default of 16 SCLK cycles (or 24 SCLK cycles if CRC is enabled), 16-bit command (1 R/W bit, 7 address bits, followed by an 8-bit data)
3. $\overline{CS}$ is pulled high

When the first bit of command is a 0 it indicates a write is being performed or when the first bit is a 1 it indicates a read is being performed. The next 7 bits following are for the target register address. The target register is determined during the 8th SCLK cycle. The last 8 bits are written to the targeted register on the 16th SCLK cycle, or they are ignored when performing a read. While performing a read the last 8 bits on SDI are ignored since SDO will output the addressed register state during these last 8 SCLK cycles. During the first eight bits of any command SPI sends out 8 alignment bits "0x25" on SDO.

7.4.2 Burst Mode

TMUXS7614D enters burst mode through a write to the burst mode enable bit in the BURST_EN register found in the Register Map. Burst mode grants the ability to send numerous SPI commands consecutively without deasserting the $\overline{CS}$ pin. While in burst mode the operation is in 16-bit frames by default or with CRC enabled 24-bit frames. The SDO pin aligns with the same response expected while in address mode- for reads SDO returns read-back values, and for writes SDO outputs 0x2500. The SCLK error behaves in a different manner to address mode. If the SCLK count is not a multiple of 16 or 24 then the SCLK error flag asserts. CRC and read/write invalid errors operate while in burst mode similarly to operation in address mode.

7.4.3 Daisy Chain Mode

Multiple TMUXS7614D can be chained together to operate similarly to a shift register. All SPI pins are shared across all devices in the chain, but the SDO pin is connected to the SDI of the next device in the chain. Daisy chain mode is entered by sending the command "0x2500". When multiple devices are configured in hardware to be in daisy chain mode the first command sent is expected to be the daisy chain mode entry command. As the first device is entering daisy chain mode it is simultaneously sending out "0x2500" to enter the next device into daisy chain mode. Once the series of devices is in daisy chain mode the CS pin will need to be pulled low to send switch state commands.

The SDO pin acts as an eight cycle delayed SDI of the same device. After all devices in the chain have received a switch state command and the CS pin is pulled high- each device will enter the switch states that were assigned to it. While in daisy chain mode all commands will only target the switch state registers so configuration registers will be unavailable. To leave daisy chain mode a power cycle will be necessary.

7.4.4 Error Detection

TMUXS7614D has robust SPI communication protocol error detection features that are covered in the following sections.

7.4.4.1 Address R/W Error Flag

When an invalid register address is the target for a read or write- an error is detected on the rising edge of the 9th SCLK cycle and asserts an error flag. Invalid registers include: writing to a read only register or a nonexistent register is targeted for either a read or a write. This is a default setting and can be configured through the R/W error enable bit in the ERR_CONFIG register.

7.4.4.2 SCLK Count Error Flag

The SCLK count error flag asserts when an incorrect number of SCLK cycles are sent to the device. In address mode the expected SCLK cycles is 16 and with CRC enabled the expected count is 24. If less than 16 (address mode) or 24 (with CRC enabled) are received then the device prevents writes to the register map. If there are more cycles than expected the write still occurs; however, an SCLK count error flag asserts. SCLK count error is enabled by default and can be configured through the SCLK count error enable bit in the ERR_CONFIG register.

7.4.4.3 CRC (Cyclic Redundancy Check) Enable and Error Flag

CRC is disabled by default and can be enabled through the CRC_ERR_EN bit in the ERR_CONFIG register. When CRC is enabled the expected SCLK cycles change from 16 to 24. The additional 8 cycles are the CRC byte that is calculated by the device from the initial 16-bits of data (R/W bit, register address [6:0], and the register data [7:0]). Writes occur on the rising edge of the 24th SCLK rising edge. The CRC polynomial used is $x^8+x^2+x^1+1$ using a value of 0 as the seed.

The CRC byte, during a SPI write, is provided by the central processing unit or microcontroller. This byte is checked before the 24th SCLK rising edge by the SPI block to confirm the CRC byte aligns with the first 16 bits received. If the CRC byte is incorrect then the register write is blocked and the CRC error flag asserts. TMUXS7614D provides the CRC byte through SDO during a SPI read.

7.4.4.4 Clearing Error Flags

To clear out the error flag register the 16-bit command 0x6CA9 must be sent to TMUXS7614D. With CRC enabled, the correct CRC byte must be provided for the error clear command to execute. On either the 16^{th} or 24^{th} SCLK rising edge (24^{th} for CRC enabled) the error flag register is cleared. 0x6CA9 does not trigger the R/$\overline{W}$ address error flag.

7.4.5 Software Reset

While in address mode, a software reset can be performed by writing the two following commands consecutively to the register 0x0B:

1. 0xA3
2. 0x05

The register values reset to default after performing a software reset.

7.5 Device Functional Modes

The TMUXS7614D has eight independently selectable single-pole, single-throw switches that are turned-on or turned-off through the SPI interface. This device can operate without any external components. This is because 0.1µF decoupling capacitors are integrated into the device for VDD, VSS, and VL.

The SPI interface features error detection, support daisy chain with multiple devices, and SPI modes 0 and 3. Additionally, the SCLK can operate at speeds up to 50MHz for SPI logic levels 2.7V to 5.5V.

ADVANCE INFORMATION

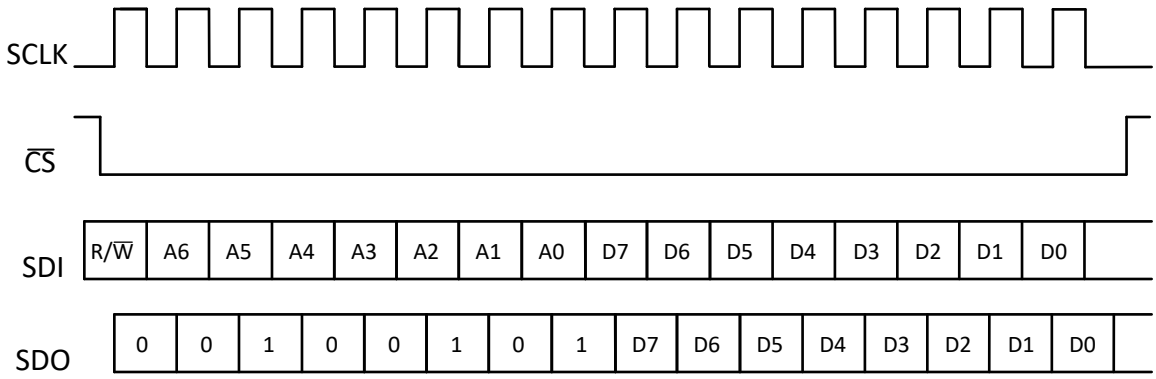

Figure 7-1. SPI Address Mode Diagram (16-bits)

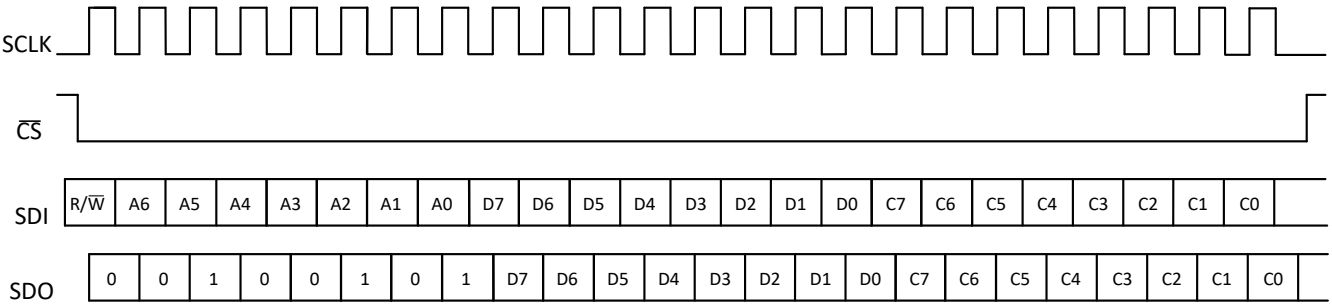

Figure 7-2. SPI Address Mode Diagram with CRC (24-bits)

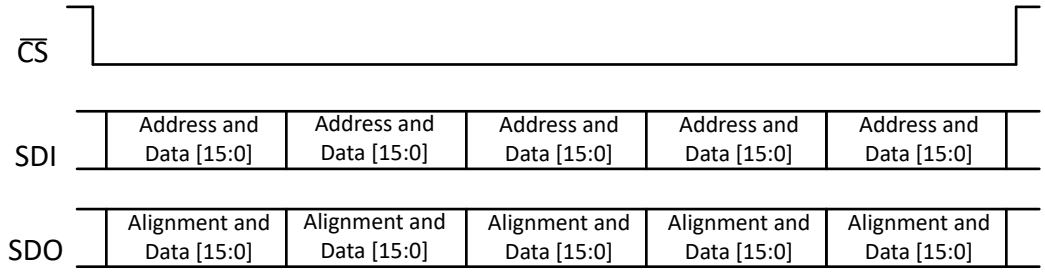

Figure 7-3. SPI Burst Mode Example

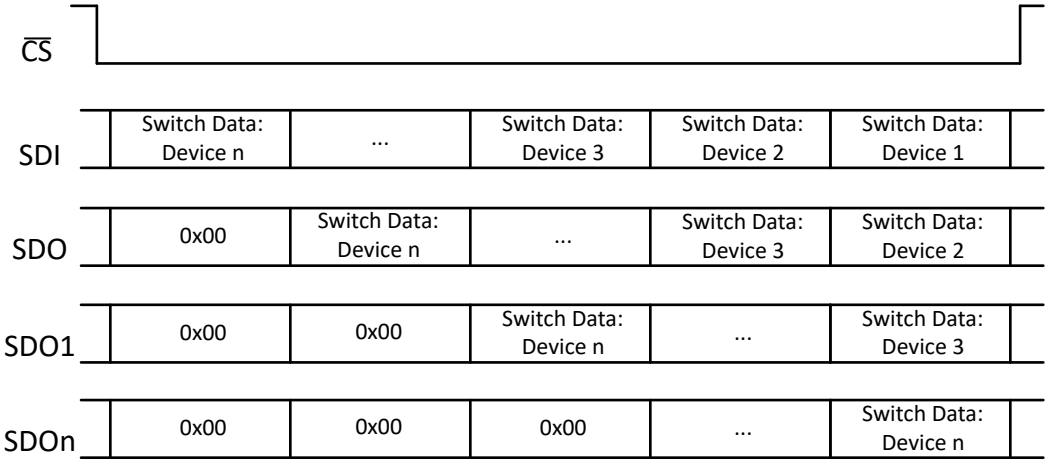

Figure 7-4. SPI Daisy Chain Mode Example

7.6 Register Map

Table 7-1.

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Permission
0x01	SW_DATA	SW8_EN	SW7_EN	SW6_EN	SW5_EN	SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/$\overline{W}$
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/$\overline{W}$
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/$\overline{W}$
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/$\overline{W}$

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUXS7614D is part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5V to ±25V), a single supply (4.5V to 42V), or asymmetric supplies (such as V_{DD} = 12V, V_{SS} = –5V), and offer true rail-to-rail input and output. The TMUXS7614D offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUXS7614D a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

The implementation of a parametric measurement unit (PMU) in the semiconductor automatic test equipment (ATE) application is one example of precision performance to take advantage of.

In automated test equipment (ATE) systems, the parametric measurement unit (PMU) is tasked to measure device (DUT) parametric information in terms of voltage and current. When measuring voltage, current is applied at the DUT pin, and the current range can be adjusted by changing the value of the internal sense resistor. Sometimes there is a need, depending on the DUT, to use even higher testing current than natively supported by the system. A 4 channel SPST switch can be used with an external higher current amplifier and resistor to achieve the flexibility. The PMU operating voltage is typically in mid voltage (up to 20V). An appropriate switch like the TMUXS7614D with a low leakage current (0.013 nA typical) works well in these applications because of it's minimal impact on measurement accuracy, and the low R_{ON} and flat $R_{ON\_FLATNESS}$ offered allows the current range to be controlled more precisely. Figure 8-1 shows simplified diagram of such implementations in memory and semiconductor test equipment.

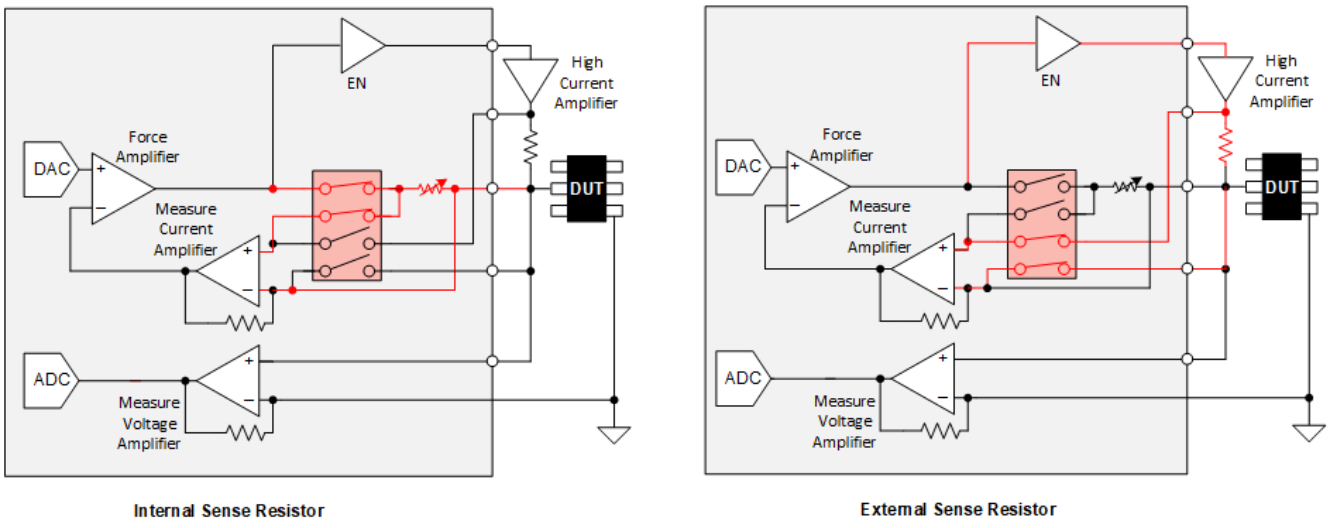


Figure 8-1. High Current Range Selection Using External Resistor

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

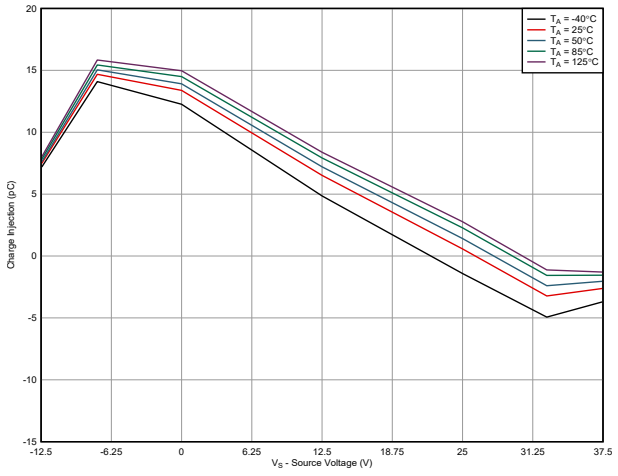
PARAMETERS	VALUES
Supply (V_{DD})	20V
Supply (V_{SS})	–10V
Input / Output signal range	–10V to 20V (Rail-to-Rail)
Control logic thresholds	1.8V compatible

8.2.2 Detailed Design Procedure

Figure 10-1 demonstrates how the TMUXS7614D can be used in semiconductor test equipment for high-precision, high-voltage, multi-channel measurement applications. The TMUXS7614D can support 1.8V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUXS7614D can operate without any external components except for the supply decoupling capacitors. The select pins have an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUXS7614D including signal range and continuous current. For this design with a positive supply of 20V on V_{DD} and negative supply of -10V on V_{SS}, the signal range can be 20V to -10V. The maximum continuous current (I_{DC}) can be up to 330mA as shown in the *Recommended Operating Conditions* table for wide-range current measurement.

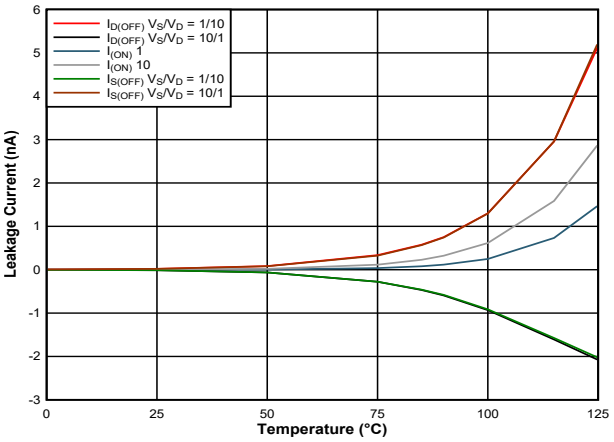
8.2.3 Application Curve

The TMUXS7614D have excellent charge injection performance and ultra-low leakage current, making them an excellent choice for minimizing sampling errors for the sample and hold application.



T_A = 25°C

Figure 8-2. Charge Injection vs. Source Voltage



V_{DD} = 15V, V_{DD} = -15V

Figure 8-3. On-Leakage vs. Source or Drain Voltage

8.3 Thermal Considerations

For analog switches in many applications, several 100mA of current needs to be supported through the switch (from source to drain, or NO/NC to COM). Many devices already have a maximum current specified based on ambient temperature, but if a device specifies with junction temperature or you want to calculate for your specific use case (temperature, supply voltage, channels in parallel) you can use the following equations and scheme.

There are mainly 2 limitations to this maximum current:

1. Inherent metal limitations of the device

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2. Thermal self-heating limitations

To calculate maximum current for your specific setup you need the following information:

- T_A = maximum ambient temperature
- $R_{\Theta JA}$ = package thermal coefficients
- R_{ON} = on resistance
- n = number of channels in parallel
- Limitations on maximum current based on junction temperature from the datasheet

Below is an example using TMUXS7614D specifications:

Device maximum T_J=150°C

$R_{\Theta JA}$=53.5 °C/W

While operating with 4 channels in parallel at ±15V, we can assume R_{ON} = 1.8Ω by taking the maximum specified value at T_A = 105°C. We will use T_J = 125°C. Using the following equation we can calculate the maximum thermal limitation.

$$I = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times R_{ON} \times n}} \quad (2)$$

The current calculated from this example is 0.227A, but due to the inherent metal limitation we must take the lower of the value calculated and the value provided in the maximum current table based on T_J in the datasheet which is 0.143A in this case. This means that we can only pass a maximum of 0.143A through each of the 4 channels in parallel.

Similarly you can calculate the T_J and total power dissipated in these examples with the following equations. Note there will be some small power dissipated from the supply current consumption of the device, which is ignored here.

$$T_J = R_{\theta JA} \times I^2 \times R_{ON} \times n + T_A \quad (3)$$

$$P_{total} = \frac{T_J - T_A}{R_{\theta JA}} \quad (4)$$

Pulse current can be calculated the same way, but using the duty cycle, d. Typically, pulse current is specified at a 10% duty cycle; however, do not exceed the maximum current provided in the pulse current table even with a shorter duty cycle.

$$I = \frac{1}{d}\sqrt{\frac{T_J - T_A}{R_{\theta JA} \times R_{ON} \times n}} \quad (5)$$

$$T_J = R_{\theta JA} \times (d \times I)^2 \times R_{ON} \times n + T_A \quad (6)$$

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8.4 Power Supply Recommendations

The TMUXS7614D device operates across a wide supply range of ±4.5V to ±25V (4.5V to 42V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12V and V_{SS} = –5V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. TMUXS7614D integrates supply decoupling capacitors so external supply decoupling capacitors at both the V_{DD}, V_L, V_{SS} pins to ground are unnecessary. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.5 Layout

8.5.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

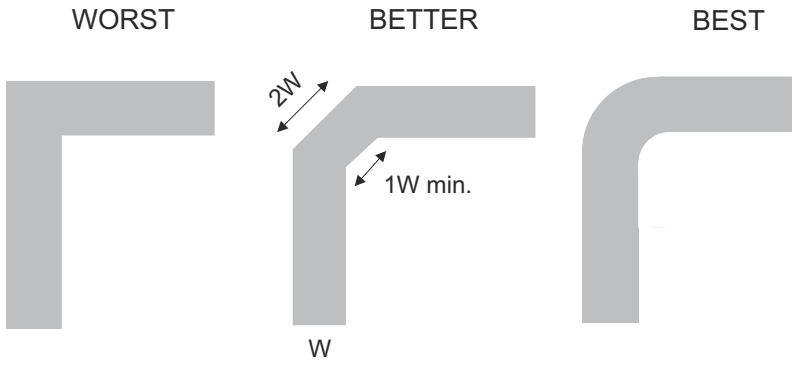

Figure 8-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points; through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

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8.5.2 Layout Example

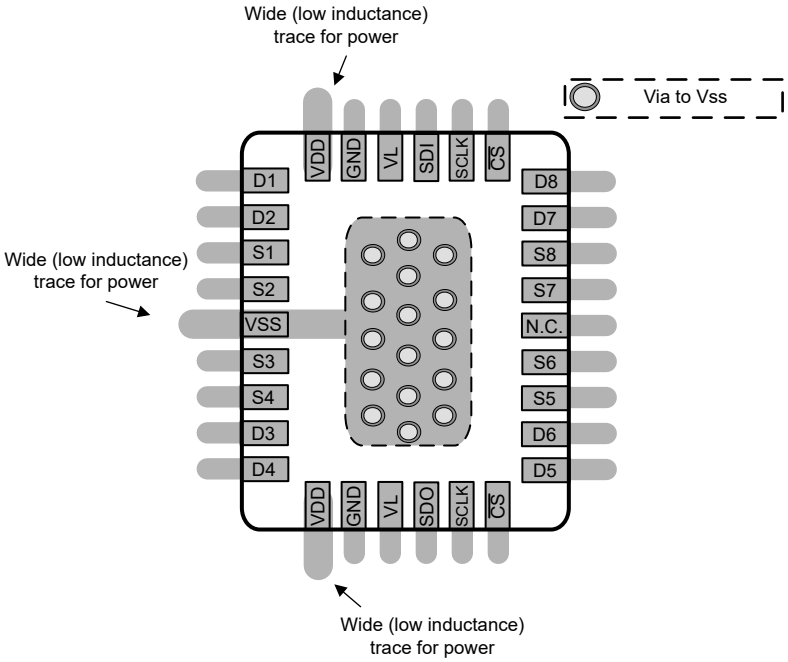

Figure 8-5. TMUXS7614D Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample and Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2024) to Revision A (July 2024)	Page
• Updates to spec tables throughout for APL	4

DATE	REVISION	NOTES
June 2024	*	Advanced Information Initial Release

ADVANCE INFORMATION

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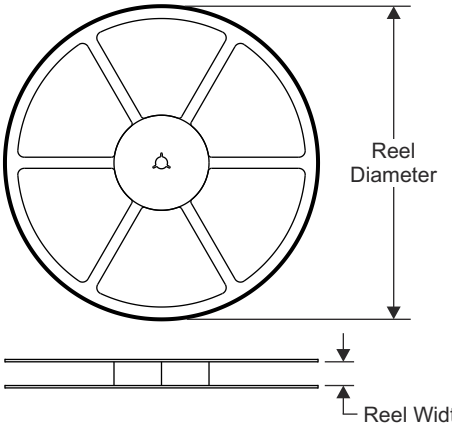
11 Mechanical, Packaging, and Orderable Information

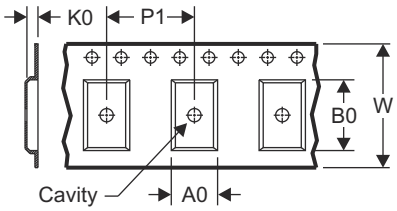
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

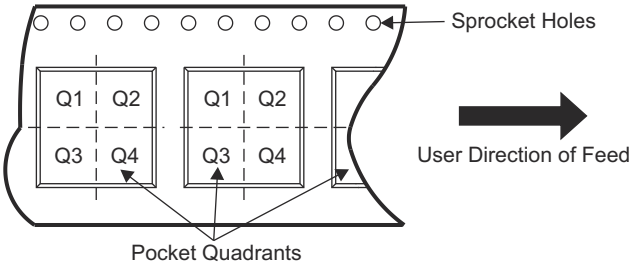


TAPE DIMENSIONS



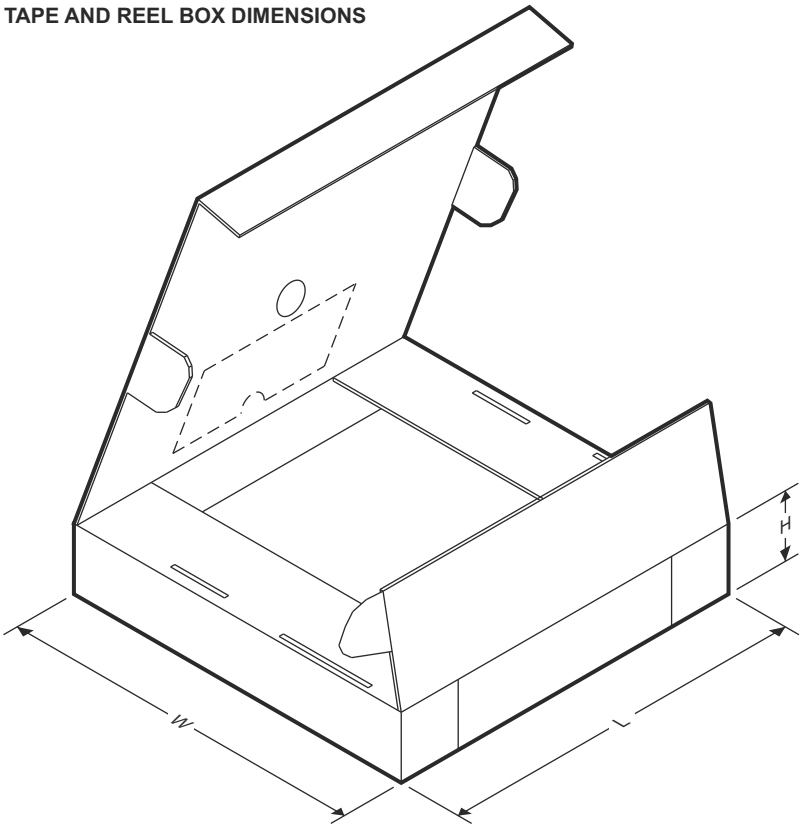
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXS7614DZEMR	FCLGA	ZEM	30	3000	330	12.4	4.35	5.35	1.3	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXS7614DZEMR	FCLGA	ZEM	30	3000	470	380	31.8

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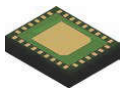
ADVANCE INFORMATION

11.2 Mechanical Data

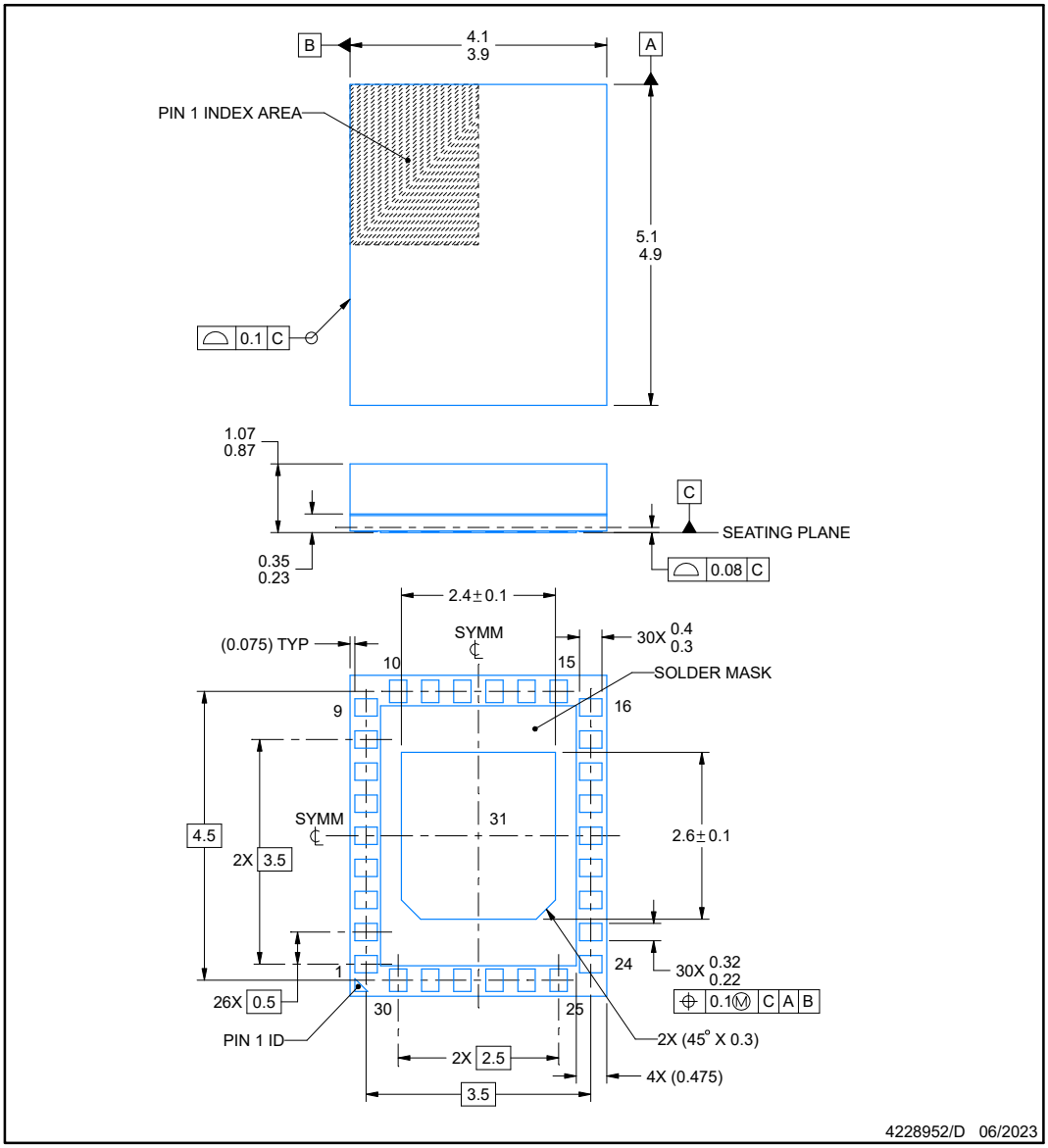
ZEM0030A



PACKAGE OUTLINE

FCLGA - 1.07 mm max height

LAND GRID ARRAY



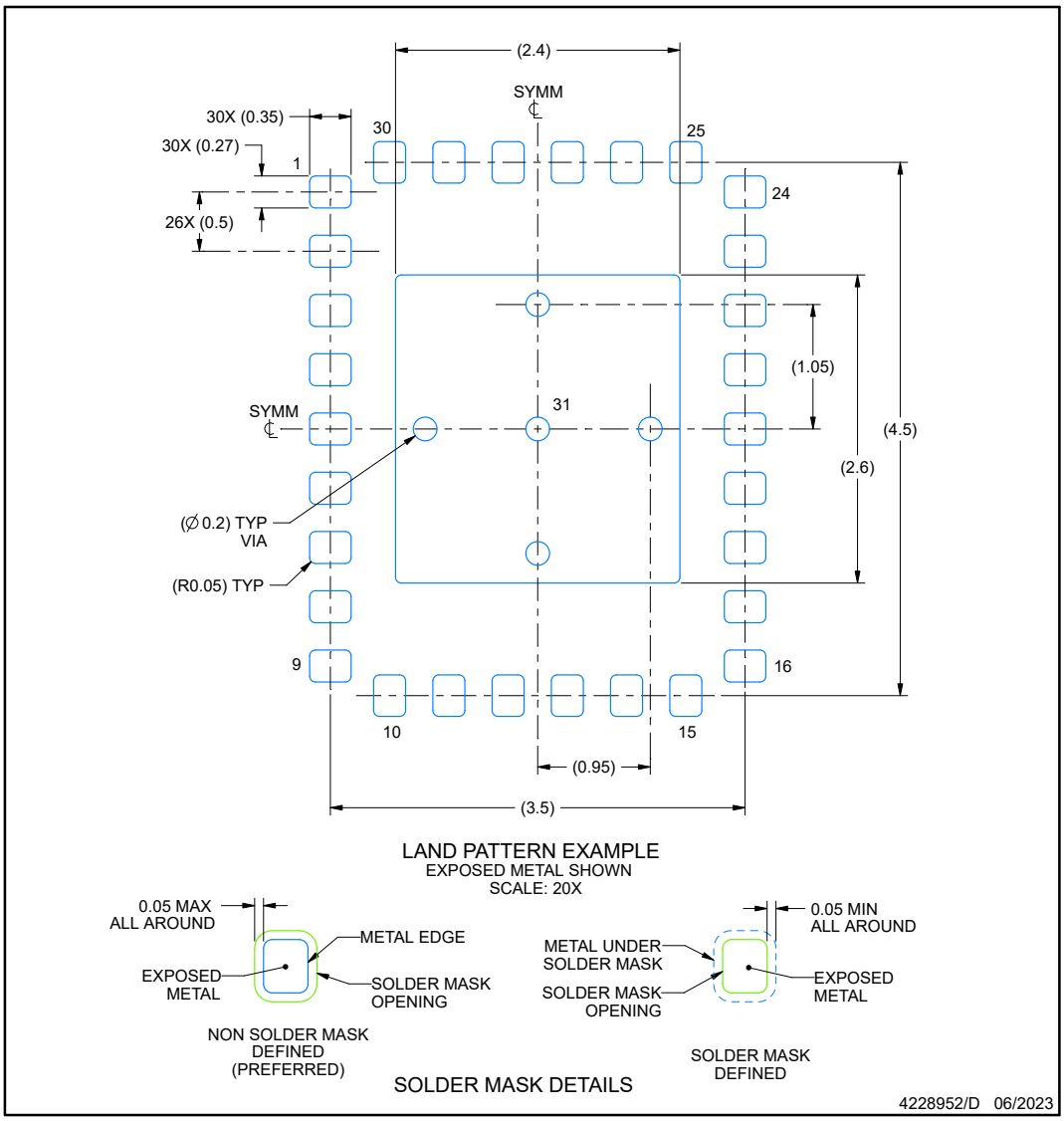
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZEM0030A — **FCLGA - 1.07 mm max height**

LAND GRID ARRAY



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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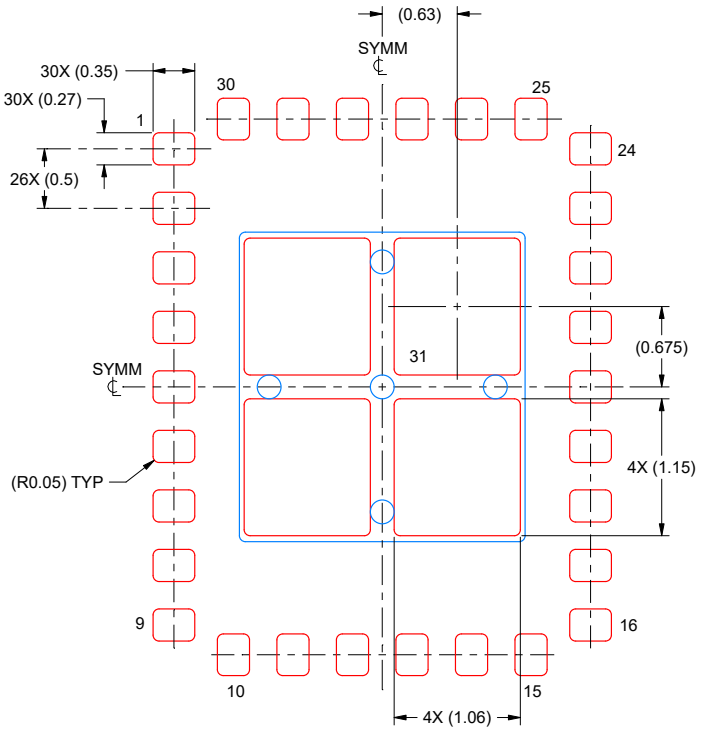
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

ZEM0030A — **FCLGA - 1.07 mm max height**

LAND GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

EXPOSED PAD 31:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228952/D 06/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUXS7614DZEMR	ACTIVE	FCLGA	ZEM	30	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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