

SNx4AHC245 Octal Bus Transceivers With 3-State Outputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points of sale

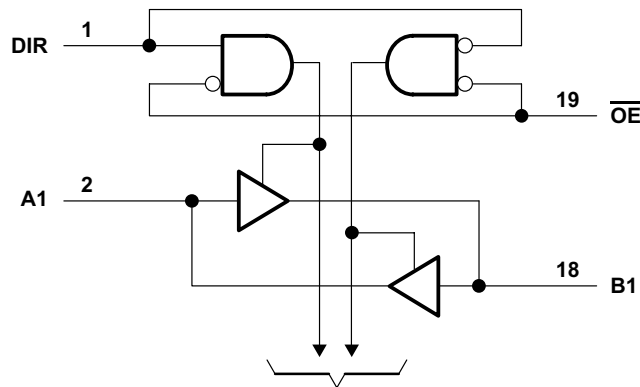
3 Description

The SNx4AHC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. This part operates from 4.5V to 5.5V.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN54AHC245	J (CDIP, 20)	24.20mm × 7.62mm	24.20mm × 6.92mm
	W (CFP, 20)	13.09mm × 8.13mm	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74AHC245	DB (SSOP, 20)	7.20mm × 7.8mm	7.20mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 6.4mm	5.00mm × 4.40mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm
	DGS (VSSOP, 20)	5.10mm × 4.9mm	5.10mm × 3.00mm
	RKS (VQFN, 20)	4.50mm × 2.50mm	4.50mm × 2.50mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels
Simplified Schematic



Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	10
2 Applications	1	7.3 Feature Description.....	10
3 Description	1	7.4 Device Functional Modes.....	10
4 Pin Configuration and Functions	3	8 Application and Implementation	11
5 Specifications	5	8.1 Application Information.....	11
5.1 Absolute Maximum Ratings	5	8.2 Typical Application.....	11
5.2 Handling Ratings.....	5	8.3 Power Supply Recommendations.....	12
5.3 Recommended Operating Conditions.....	5	8.4 Layout.....	12
5.4 Thermal Information.....	6	9 Device and Documentation Support	14
5.5 Electrical Characteristics.....	6	9.1 Receiving Notification of Documentation Updates....	14
5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	9.2 Support Resources.....	14
5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	7	9.3 Trademarks.....	14
5.8 Noise Characteristics.....	7	9.4 Electrostatic Discharge Caution.....	14
5.9 Operating Characteristics.....	8	9.5 Glossary.....	14
5.10 Typical Characteristics.....	8	10 Revision History	14
6 Parameter Measurement Information	9	11 Mechanical, Packaging, and Orderable Information	14
7 Detailed Description	10		
7.1 Overview.....	10		

4 Pin Configuration and Functions

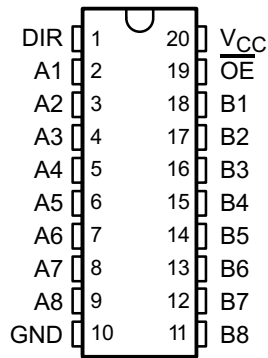


Figure 4-1. SN54AHC245 J or W, SN74AHC245 DB, DGV, DW, N, PW or DGS Package, CDIP, CFP, SSOP, TVSOP, SOIC, PDIP, TSSOP, or VSSOP 20-Pin (Top View)

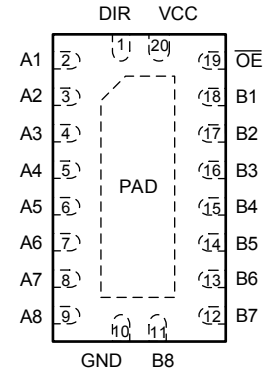


Figure 4-2. SN74AHC245 RKS Package, VQFN 20-Pin (Top View)

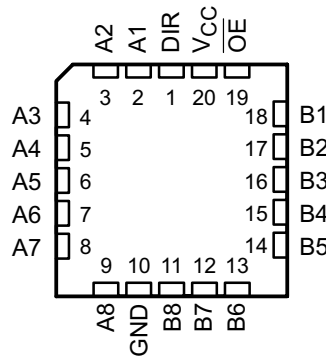


Figure 4-3. SN54AHC245 FK Package, LCCC 20-Pin (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DIR	1	I/O	Direction Pin
A1	2	I/O	A1 Input/Output
A2	3	I/O	Y4 Input/Output
A3	4	I/O	A2 Input/Output
A4	5	I/O	Y3 Input/Output
A5	6	I/O	A3 Input/Output
A6	7	I/O	Y2 Input/Output
A7	8	I/O	A4 Input/Output
A8	9	I/O	Y1 Input/Output
GND	10	—	Ground Pin
B8	11	I/O	A1 Input/Output
B7	12	I/O	Y4 Input/Output
B6	13	I/O	A2 Input/Output
B5	14	I/O	Y3 Input/Output
B4	15	I/O	A3 Input/Output
B3	16	I/O	Y2 Input/Output
B2	17	I/O	A4 Input/Output

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
B1	18	I/O	Y1 Input/Output
$\overline{OE}$	19	I/O	Output Enable
V _{CC}	20	—	Power Pin
Thermal pad		—	Thermal Pad ⁽²⁾

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

(2) RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range ⁽¹⁾	Control inputs	−0.5	7	V
V_O	I/O, Output voltage range		−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ Control inputs		−20	mA
I_{OK}	I/O, Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54AHC245		SN74AHC245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage	OE or DIR	0	5.5	0	5.5	V
V_O	Output voltage	A or B	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		−4		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DB	DGV	DW	N	NS	PW	RGY	RKS	DGS	UNIT
		20 PINS									
R _{θJA}	Junction-to-ambient thermal resistance	113.1	116.1	96.2	51.5	77.1	122.3	35.1	67.7	118.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.9	31.3	63.6	38.2	43.6	64.8	43.3	72.4	57.7	
R _{θJB}	Junction-to-board thermal resistance	67.9	57.6	64.7	32.4	44.6	73.3	12.9	40.4	73.1	
Ψ _{JT}	Junction-to-top characterization parameter	39.3	1.0	40.5	24.6	17.2	19	0.9	10.3	5.7	
Ψ _{JB}	Junction-to-board characterization parameter	67.5	56.9	64.3	32.3	44.2	73	12.9	40.4	72.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	7.9	24.1	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	V _I = V _{CC} or GND	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA		3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA		4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	V _I = V _{CC} or GND	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA		3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA		4.5 V			0.36		0.5		0.44	
I _I	A or B inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
	OE or DIR		0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1	
I _{OZ} ⁽²⁾		V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
C _i	OE or DIR	V _I = V _{CC} or GND	5 V			2.5				10	pF
C _{io}	A or B inputs	V _I = V _{CC} or GND	5 V			4					pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) The parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	C _L = 15 pF		5.8 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns
t _{PHL}					5.8 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	
t _{PZH}	OE	A or B	C _L = 15 pF		8.5 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	ns
t _{PZL}					8.5 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	
t _{PHZ}	OE	A or B	C _L = 15 pF		8.9 ⁽¹⁾	12.5 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	ns
t _{PLZ}					8.9 ⁽¹⁾	12.5 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	

5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	$C_L = 50\text{ pF}$	8.3	11.9		1	13.5	1	13.5	ns
t_{PHL}				8.3	11.9		1	13.5	1	13.5	
t_{PZH}	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	11	16.7		1	19	1	19	ns
t_{PZL}				11	16.7		1	19	1	19	
t_{PHZ}	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	11.5	15.8		1	18	1	18	ns
t_{PLZ}				11.5	15.8		1	18	1	18	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5 ⁽²⁾					1.5	ns

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	$C_L = 15\text{ pF}$	4 ⁽¹⁾	5.5 ⁽¹⁾		1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	ns
t_{PHL}				4 ⁽¹⁾	5.5 ⁽¹⁾		1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	
t_{PZH}	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$	5.8 ⁽¹⁾	8.5 ⁽¹⁾		1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns
t_{PZL}				5.8 ⁽¹⁾	8.5 ⁽¹⁾		1 ⁽¹⁾	10 ⁽¹⁾	1	10	
t_{PHZ}	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$	5.6 ⁽¹⁾	7.8 ⁽¹⁾		1 ⁽¹⁾	9.2 ⁽¹⁾	1	9.2	ns
t_{PLZ}				5.6 ⁽¹⁾	7.8 ⁽¹⁾		1 ⁽¹⁾	9.2 ⁽¹⁾	1	9.2	
t_{PLH}	A or B	B or A	$C_L = 50\text{ pF}$	5.5	7.5		1	8.5	1	8.5	ns
t_{PHL}				5.5	7.5		1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	7.3	10.6		1	12	1	12	ns
t_{PZL}				7.3	10.6		1	12	1	12	
t_{PHZ}	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	7	9.7		1	11	1	11	ns
t_{PLZ}				7	9.7		1	11	1	11	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 ⁽²⁾					1	ns

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

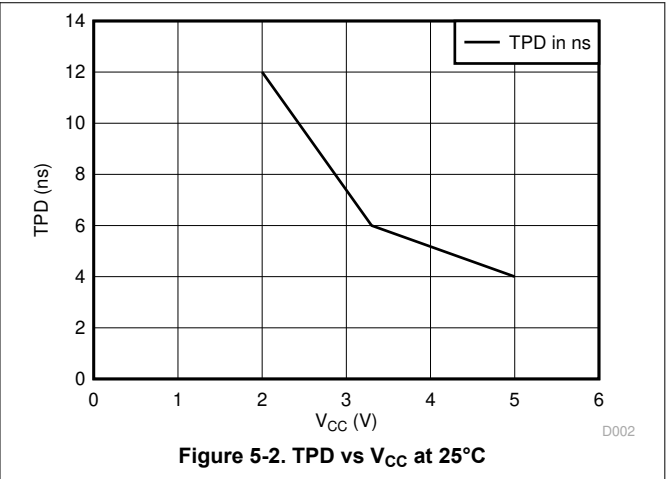
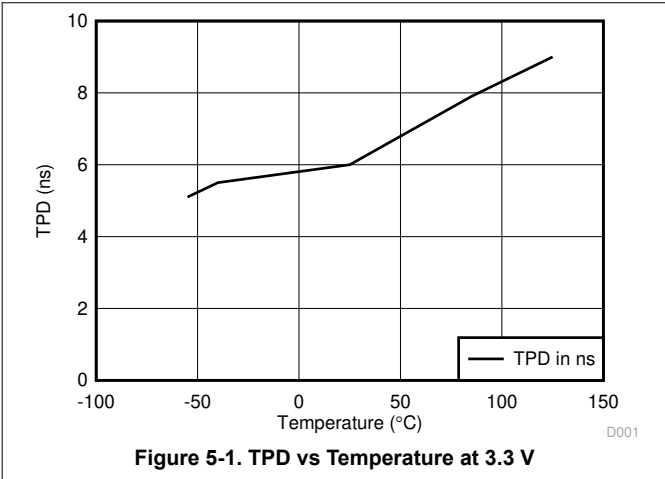
- (1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

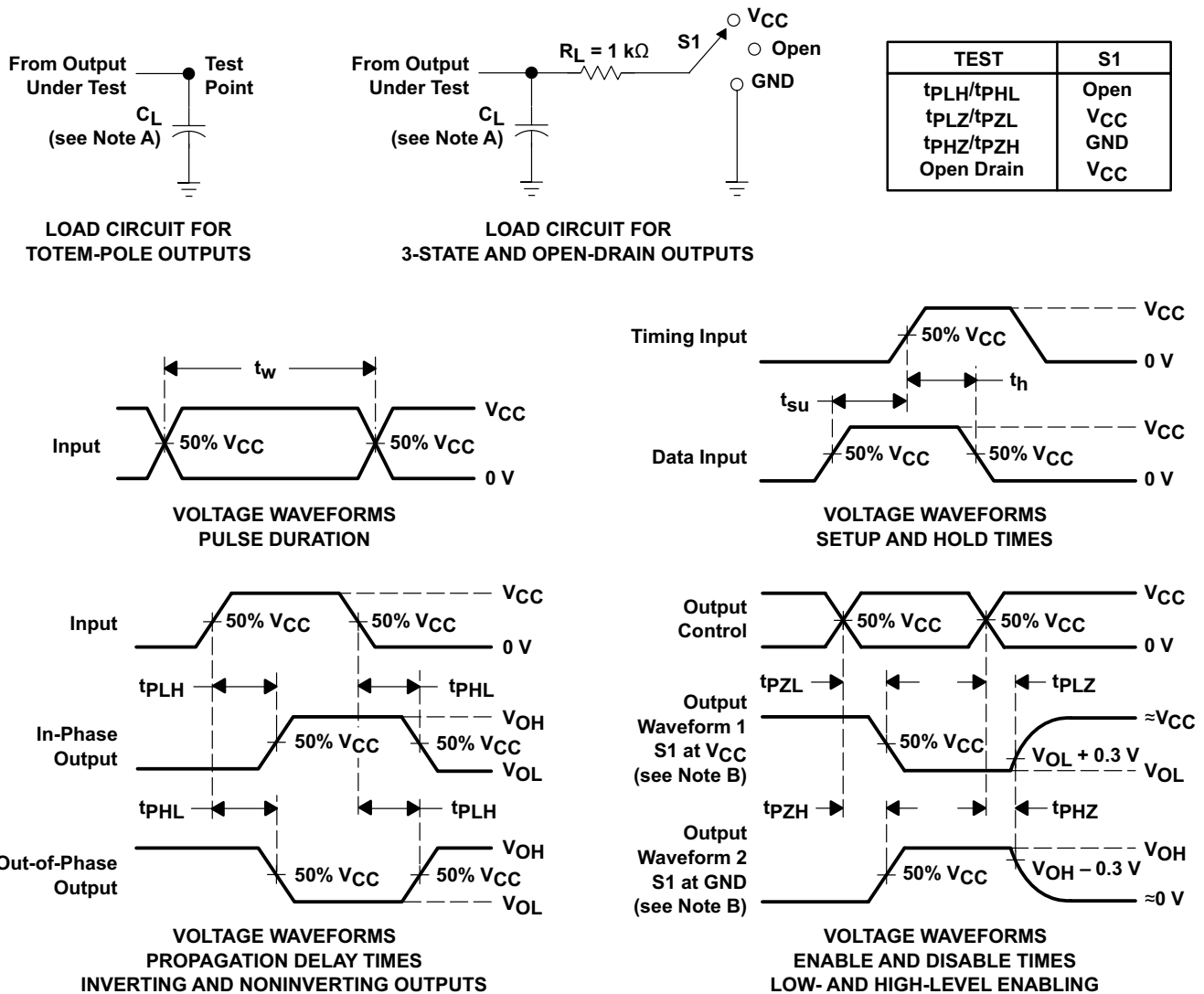
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	$f = 1\text{ MHz}$	14	pF

5.10 Typical Characteristics



6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

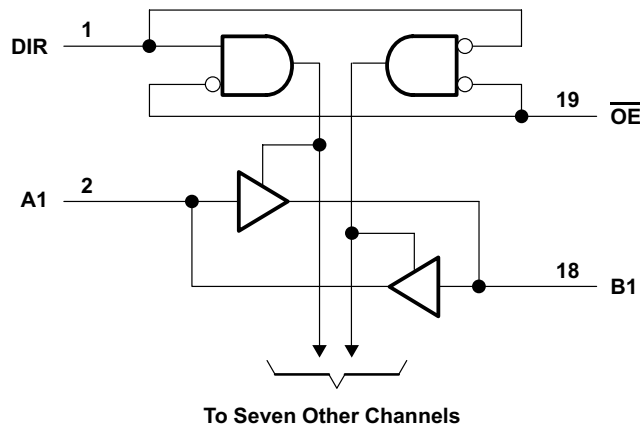
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4AHC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. For the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows down voltage translation from 5 V to 3.3 V
 - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

7.4 Device Functional Modes

**Table 7-1. Function Table
(Each Transceiver)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AHC245A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it ideal for down translation.

8.2 Typical Application

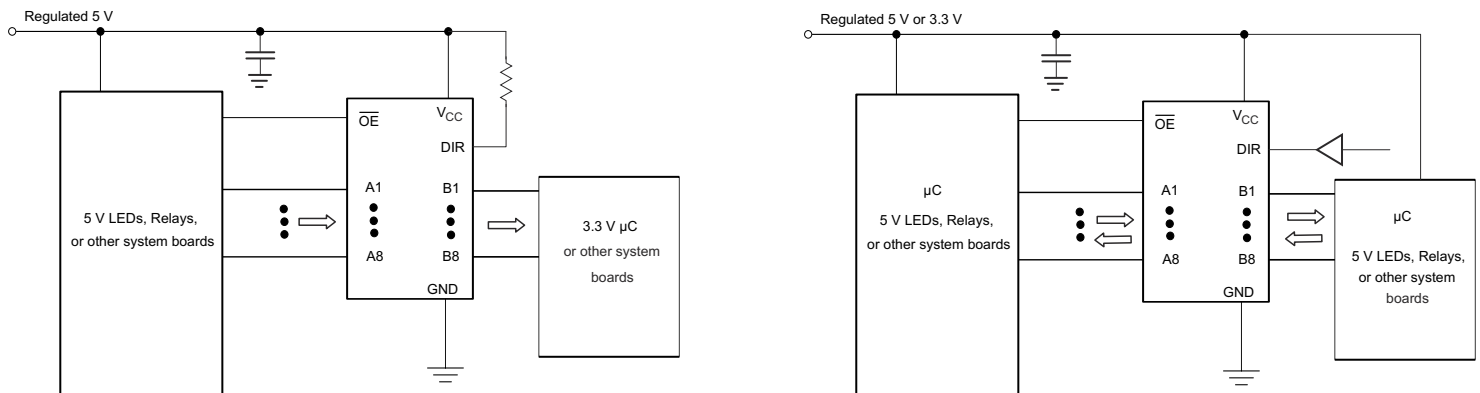


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves

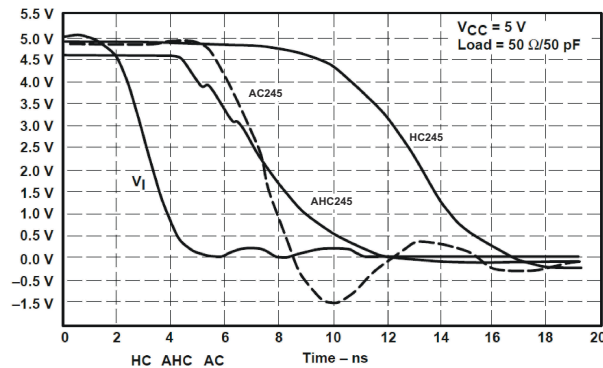


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.4.2 Layout Example

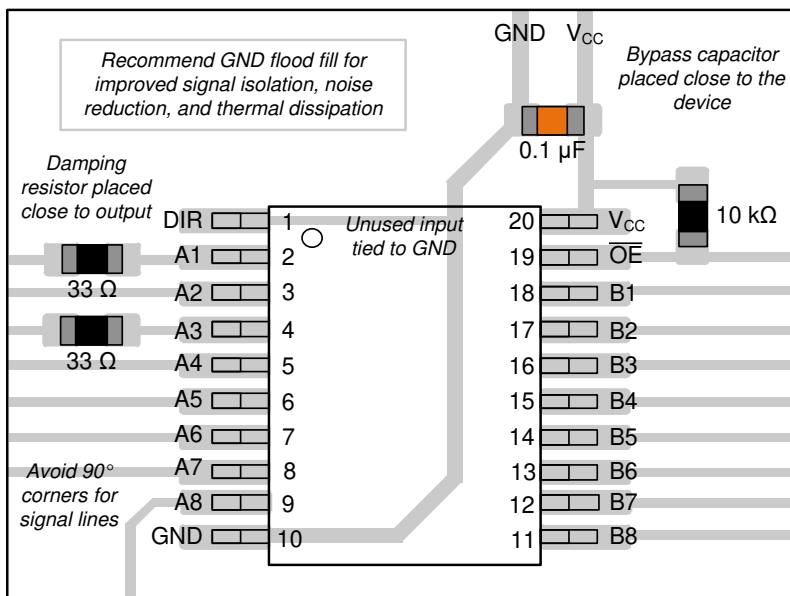


Figure 8-3. Example Layout of the SN74AHC245

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (June 2023) to Revision N (June 2024)	Page
• Added package size to <i>Device Information</i> table.....	1
• Updated names in <i>Pin Functions</i> table.....	3
• Updated <i>Layout Example</i>	13

Changes from Revision L (April 2023) to Revision M (June 2023)	Page
• Updated RθJA values: DB = 96.0 to 113.1, DW = 79.8 to 96.2, PW = 102.8 to 122.3; Updated DB, DW, and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9681801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK	Samples
5962-9681801QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QR A SNJ54AHC245J	Samples
5962-9681801QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QS A SNJ54AHC245W	Samples
5962-9681801VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801VS A SNV54AHC245W	Samples
SN74AHC245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	Samples
SN74AHC245DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	Samples
SN74AHC245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	Samples
SN74AHC245DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	Samples
SN74AHC245N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC245N	Samples
SN74AHC245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	Samples
SN74AHC245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	Samples
SN74AHC245PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	Samples
SN74AHC245PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	Samples
SN74AHC245RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	Samples
SNJ54AHC245FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC245J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QR A SNJ54AHC245J	Samples
SNJ54AHC245W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QS A SNJ54AHC245W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC245, SN54AHC245-SP, SN74AHC245 :

- Catalog : [SN74AHC245](#), [SN54AHC245](#)
- Automotive : [SN74AHC245-Q1](#), [SN74AHC245-Q1](#)
- Enhanced Product : [SN74AHC245-EP](#), [SN74AHC245-EP](#)
- Military : [SN54AHC245](#)
- Space : [SN54AHC245-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated