

TCA9517-Q1 Level-Shifting I²C Bus Repeater

1 Features

- AEC-Q100 Qualified for automotive applications
 - Device temperature: -40°C to 125°C T_A
 - Device HBM classification Level: $\pm 5500\text{-V}$
 - Device CDM classification Level: $\pm 1000\text{-V}$
- [Functional Safety-Capable](#)
 - [Documentation available to aid functional safety system design](#)
- Two-channel bidirectional buffer
- I²C Bus and SMBus compatible
- Operating Supply Voltage Range of 0.9-V to 5.25-V on A-side
- Operating supply voltage range of 2.7-V to 5.25-V on B-side
- Voltage-level translation from 0.9-V to 5.25-V and 2.7-V to 5.25-V
- Active-high repeater-enable input
- Open-drain I²C I/O
- 5.25-V tolerant I²C and enable input support mixed-mode signal operation
- Accommodates standard mode and fast mode I²C devices and multiple controller
- High-impedance I²C pins when powered-off
- Latch-up performance exceeds 100 mA Per JESD 78, class II

2 Applications

- [Servers](#)
- [Routers \(telecom switching equipment\)](#)
- [Industrial equipment](#)
- Products with Many I²C targets and/or long PCB traces

3 Description

The TCA9517-Q1 is a bidirectional buffer with level shifting capabilities for I²C and SMBus systems. It supplies bidirectional voltage-level translation (up-translation and/or down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.25 V) in mixed-mode applications. This device enables I²C and SMBus systems to be extended without loss of performance, even during level shifting.

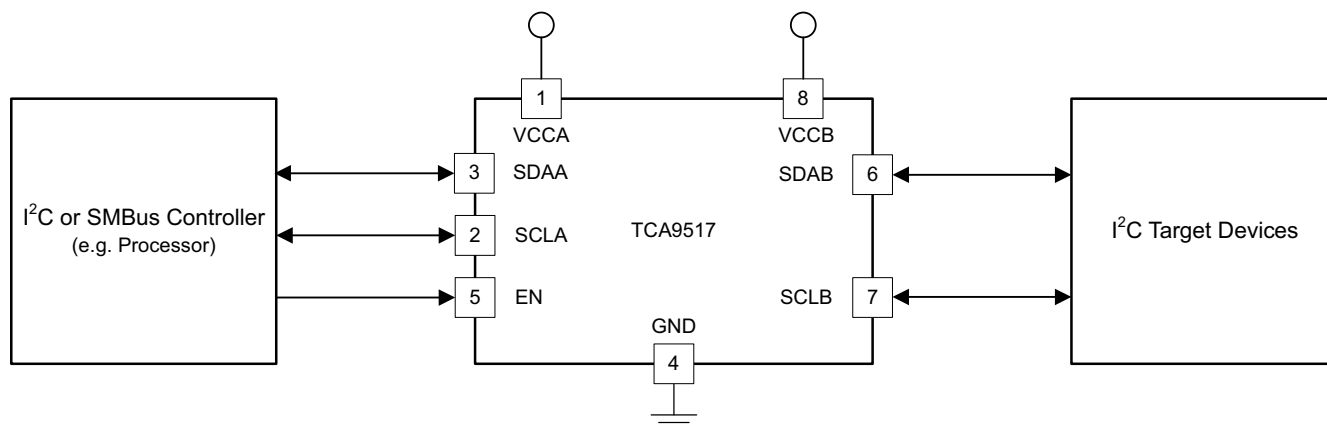
The TCA9517-Q1 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I²C application.

The TCA9517-Q1 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are overvoltage tolerant to 5.25 V, even when the device is unpowered (V_{CCB} and/or $V_{CCA} = 0\text{ V}$).

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|-------------------|
| TCA9517-Q1 | VSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (June 2018) to Revision A (February 2022) | Page |
|---|------|
| • Changed all instances of legacy terminology to controller and target where mentioned..... | 1 |
| • Added <i>Feature</i> "Functional Safety-Capable"..... | 1 |

5 Description (continued)

The buffer design on the B-side prevents its use in series with devices that use static voltage offset. The devices do not recognize buffered low signals as a valid low, and do not propagate it as a buffered low again.

The B-side drivers operate from 2.7 V to 5.25 V. The output low level for this internal buffer is approximately 0.5 V. The input voltage must be more than 70 mV below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

The A-side drivers operate from 0.9 V to 5.25 V, and drive more current. They do not require the buffered low feature (or the static offset voltage). A low signal on the B-side translates to a nearly 0 V low on the A-side. This accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A-side drives a hard low. The input level is set at $0.3 \times V_{CCA}$ to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A-side of two or more TCA9517-Q1 devices can be connected together. This allows many topographies (See [Figure 8](#) and [Figure 9](#)) with the A-side as the common bus. The A-side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple TCA9517-Q1 devices can be connected in series, A-side to B-side, with no buildup in offset voltage, and with only time-of-flight delays to consider. The TCA9517-Q1 cannot be connected B-side to B-side, because of the buffered low voltage from the B-side. The B-side cannot be connected to a device with rise time accelerators.

V_{CCA} is only used to provide the $0.3 \times V_{CCA}$ reference to the A-side input comparators and for the power-good-detect circuit. The TCA9517-Q1 logic and all I/Os are powered by the VCCB pin.

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The TCA9517-Q1 has standard open-drain configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA in a generic I²C system, where Standard mode devices and multiple controllers are possible. Higher termination currents can be used in some cases.

6 Pin Configuration and Functions

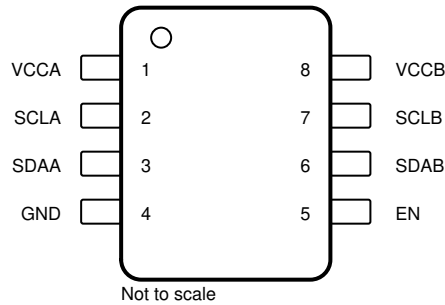


Figure 6-1. DGK (VSSOP) Package, 8-Pin, Top View

Table 6-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|------|--------------|---|
| NO. | NAME | | |
| 1 | VCCA | Supply | A-side supply voltage (0.9 V to 5.25 V) |
| 2 | SCLA | Input/Output | Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground. |
| 3 | SDAA | Input/Output | Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground. |
| 4 | GND | Ground | Ground |
| 5 | EN | Input | Active-high repeater enable input |
| 6 | SDAB | Input/Output | Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground. |
| 7 | SCLB | Input/Output | Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground. |
| 8 | VCCB | Supply | B-side and device supply voltage (2.7 V to 5.25 V) |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|------|------|------|
| V _{CCB} | Supply voltage range | -0.5 | 7 | V |
| V _{CCA} | Supply voltage range | -0.5 | 7 | V |
| V _I | Enable input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V _{I/O} | I ² C bus voltage range ⁽²⁾ | -0.5 | 7 | V |
| I _{IK} | Input clamp current | | -50 | mA |
| I _{OK} | Output clamp current | | -50 | |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±5500 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |
| | | Machine model (A115-A) | ±200 |

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--------------------------------|-------------------------------------|------------------------|------|
| V _{CCA} | Supply voltage, A-side bus | 0.9 ⁽²⁾ | 5.25 | V |
| V _{CCB} | Supply voltage, B-side bus | V _{CCA} ≤ V _{CCB} | 2.7 | 5.25 |
| | | V _{CCA} > V _{CCB} | 2.9 | 5.25 |
| V _{IH} | High-level input voltage | SDAA, SCLA | 0.7 × V _{CCA} | 5.25 |
| | | SDAB, SCLB | 0.7 × V _{CCB} | 5.25 |
| | | EN | 0.7 × V _{CCB} | 5.25 |
| V _{IL} | Low-level input voltage | SDAA, SCLA | 0.3 × V _{CCA} | V |
| | | SDAB, SCLB ⁽¹⁾ | 0.3 × V _{CCB} | |
| | | EN | 0.3 × V _{CCB} | |
| I _{OL} | Low-level output current | | 6 | mA |
| T _A | Operating free-air temperature | -40 | 125 | °C |

- (1) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILC} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See [Section 10.2.2.2](#) for V_{ILC} application information
- (2) Low-level supply voltage

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TCA9517-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | DGK (VSSOP) | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 187.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 59.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 108.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 3.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 106.9 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

$V_{CCB} = 2.7\text{ V to }5.25\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCB} | MIN | TYP | MAX | UNIT | | |
|--------------------|--|--|-----------------|------|------|----------------------------------|---------|---------------|----|
| V_{IK} | Input clamp voltage | $I_I = -18\text{ mA}$ | 2.7 V to 5.25 V | | | -1.2 | V | | |
| V_{OL} | Low-level output voltage | SDAB, SCLB $I_{OL} = 100\text{ }\mu\text{A or }6\text{ mA}$, $V_{ILA} = V_{ILB} = 0\text{ V}$ | 2.7 V to 5.25 V | 0.45 | 0.52 | 0.6 | V | | |
| | | SDAA, SCLA $I_{OL} = 6\text{ mA}$ | | | 0.1 | 0.2 | | | |
| $V_{OL} - V_{ILC}$ | Low-level input voltage below low-level output voltage | SDAB, SCLB ensured by design | 2.7 V to 5.25 V | | 70 | | mV | | |
| V_{ILC} | SDA and SCL low-level input voltage contention | SDAB, SCLB | 2.7 V to 5.25 V | | 0.4 | | V | | |
| I_{CC} | Quiescent supply current for V_{CCA} | Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND | | | | 1 | mA | | |
| I_{CC} | Quiescent supply current | Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB} | 5.25 V | | 1.5 | 5 | mA | | |
| | | Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open | | | 1.5 | 5 | | | |
| | | In contention, SDAA = SCLA = GND and SDAB = SCLB = GND | | | 3 | 5 | | | |
| I_I | Input leakage current | SDAB, SCLB | 2.7 V to 5.25 V | | | $V_I = V_{CCB}$ | ± 1 | μA | |
| | | | | | | $V_I = 0.2\text{ V}$ | 10 | | |
| | | SDAA, SCLA | | | | $V_I = V_{CCB}$ | ± 1 | | |
| | | | | | | $V_I = 0.2\text{ V}$ | 10 | | |
| | | EN | | | | $V_I = V_{CCB}$ | ± 1 | | |
| | | | | | | $V_I = 0.2\text{ V}$ | -10 -30 | | |
| I_{OH} | High-level output leakage current | SDAB, SCLB | 2.7 V to 5.25 V | | | $V_O = 3.6\text{ V}$ | 10 | μA | |
| | | SDAA, SCLA | | | | $V_O = 3.6\text{ V}$ | 10 | | |
| C_I | Input capacitance | EN | 3.3 V | | | $V_I = 3\text{ V or }0\text{ V}$ | 6 | 10 | pF |
| | | SCLA, SCLB | | | | $V_I = 3\text{ V or }0\text{ V}$ | 8 | 13 | |
| | | | | | | $V_I = 0\text{ V}$ | 7 | 11 | |
| C_{IO} | Input/output capacitance | SDAA, SDAB | 3.3 V | | | 8 | 13 | pF | |
| | | | 0 V | | | 7 | 11 | | |

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| t_{su} Setup time, EN high before Start condition ⁽¹⁾ | 100 | | ns |
| t_h Hold time, EN high after Stop condition ⁽¹⁾ | 100 | | ns |

(1) EN should change state only when the global bus and the repeater port are in an idle state.

7.7 I²C Interface Switching Characteristics

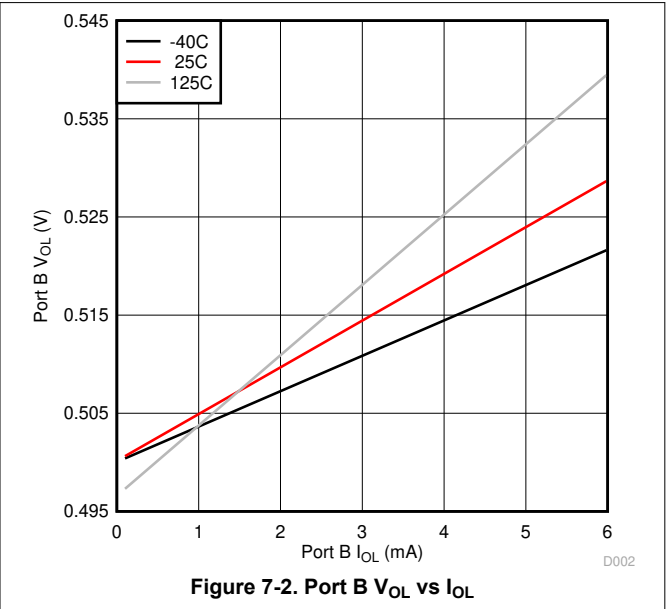
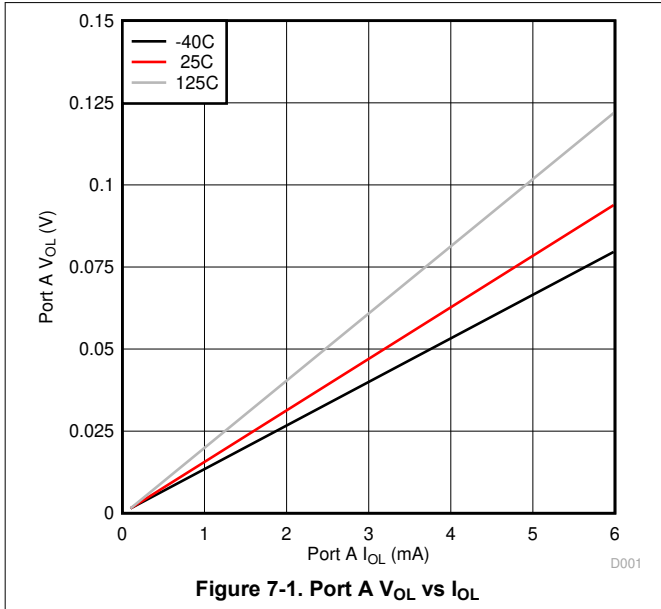
$V_{CCB} = 2.7\text{ V to }5.25\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)^{(1) (4)}

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP ⁽⁵⁾ | MAX | UNIT |
|------------------|--------------------------------------|---|---|---|-----|--------------------|-----|------|
| t _{PLZ} | Propagation delay | SDAB, SCLB ⁽³⁾ (see Figure 8-4) | SDAA, SCLA ⁽³⁾ (see Figure 8-4) | | | 141 | 250 | ns |
| | | SDAA, SCLA ⁽²⁾ (see Figure 8-3) | SDAB, SCLB ⁽²⁾ (see Figure 8-3) | | | 74 | 110 | |
| t _{PZL} | Propagation delay | SDAB, SCLB | SDAA, SCLA | $V_{CCA} \leq 2.7\text{ V}$ (see Figure 8-2) | | 76 ⁽⁶⁾ | 110 | ns |
| | | | | $V_{CCA} \geq 3\text{ V}$ (see Figure 8-2) | | 95 | 290 | |
| | | SDAA, SCLA ⁽²⁾ (see Figure 8-3) | SDAB, SCLB ⁽²⁾ (see Figure 8-3) | | | 107 | 230 | |
| t _{TLH} | Transition time | 80% | 20% | $V_{CCA} \leq 2.7\text{ V}$ (see Figure 8-3) | | 12 | | ns |
| | | | | $V_{CCA} \geq 3\text{ V}$ (see Figure 8-3) | | 42 | | |
| | A side to B-side (see Figure 8-2) | | | | | 125 | | |
| t _{THL} | Transition time | 80% | 20% | $V_{CCA} \leq 2.7\text{ V}$ (see Figure 8-3) | | 67 ⁽⁶⁾ | 200 | ns |
| | | | | $V_{CCA} \geq 3\text{ V}$ (see Figure 8-3) | | 86 | 240 | |
| | | A side to B-side (see Figure 8-2) | | | | 48 | 120 | |

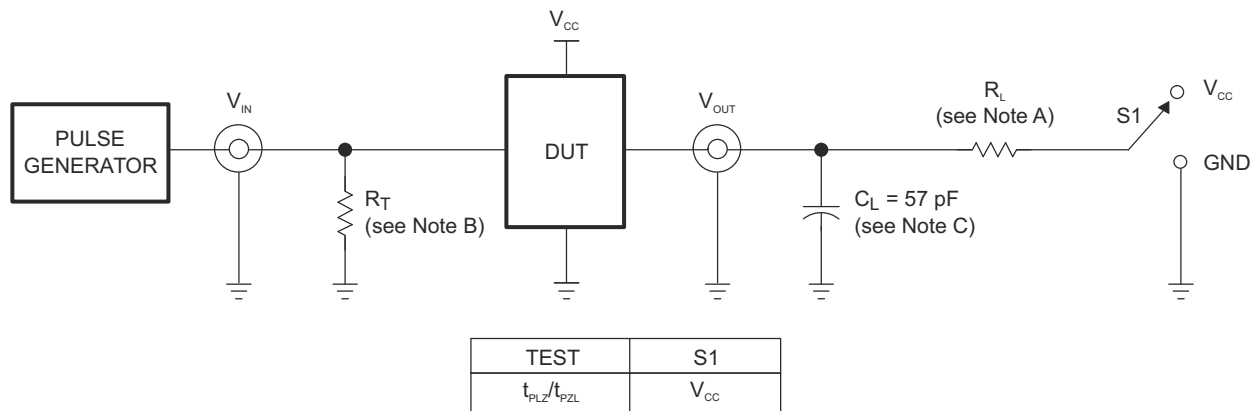
- (1) Times are specified with loads of 1.35-k Ω pull-up resistance and 50-pF load capacitance on the B-side. On the A side, for $0.9\text{-V} \leq V_{CCA} \leq 2.7\text{-V}$, a 167- Ω pull-up and 57-pF load capacitance. For $V_{CCA} \geq 3.0\text{-V}$, a 450- Ω pull-up and 57-pF load capacitance. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
- (2) The proportional delay data from A to B-side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B-side.
- (3) The t_{PLH} delay data from B to A side is measured at 0.4 V on the B-side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
- (4) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
- (5) Typical values were measured with $V_{CCA} = V_{CCB} = 3.3\text{ V}$ at $T_A = 25^\circ\text{C}$, unless otherwise noted.
- (6) Typical value measured with $V_{CCA} = 2.7\text{ V}$ at $T_A = 25^\circ\text{C}$

7.8 Typical Characteristics

$V_{CCA} = 0.9\text{ V}$, $V_{CCB} = 2.7\text{ V}$



8 Parameter Measurement Information



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

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- A. $R_L = 167 \Omega$ (0.9 V to 2.7 V) and $R_L = 450 \Omega$ (3.0 V to 5.25 V) on the A side and 1.35 k Ω on the B-side
- B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
- C. C_L includes probe and jig capacitance. $C_L = 50$ pF when on the B-side.
- D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.
- E. The outputs are measured one at a time, with one transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- H. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 8-1. Test Circuit

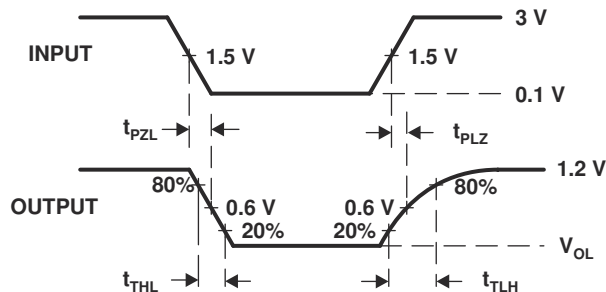


Figure 8-2. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

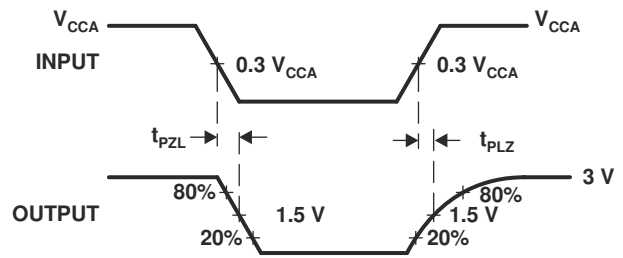


Figure 8-3. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

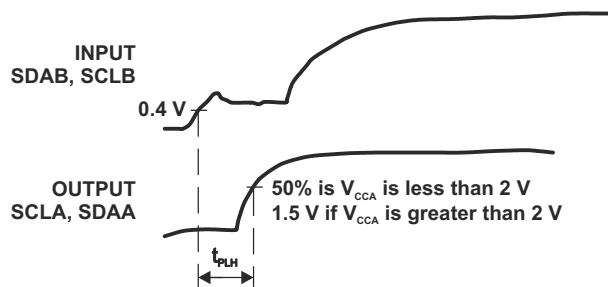


Figure 8-4. Waveform 3 – Propagation Delay for B-side to A-side

9 Detailed Description

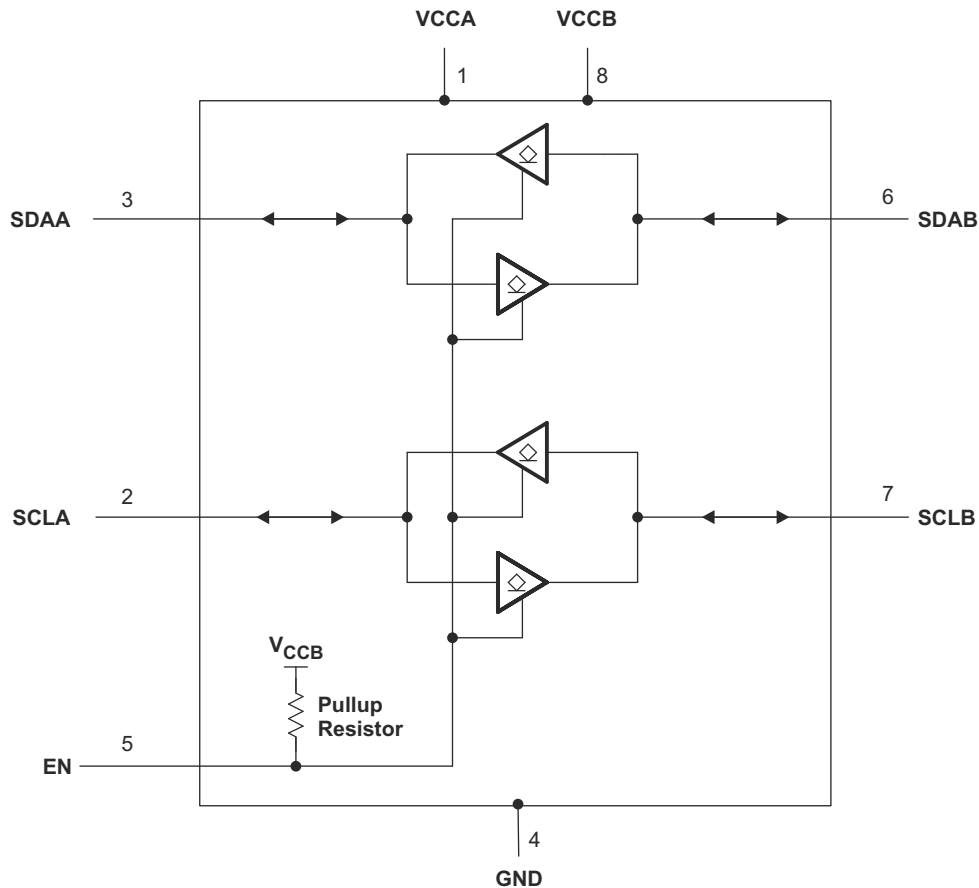
9.1 Overview

The TCA9517-Q1 is a bidirectional buffer with level shifting capabilities for I²C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.25 V) in mixed-mode applications. This device enables I²C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517-Q1 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I²C application.

The TCA9517-Q1 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.25 V, even when the device is unpowered (V_{CCB} and/or $V_{CCA} = 0$ V).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517-Q1 is a two-channel bidirectional buffer with level-shifting capabilities

9.3.2 Active-High Repeater-Enable Input

The TCA9517-Q1 has an active-high enable (EN) input with an internal pull-up to V_{CCB} , which allows the user to select when the repeater is active. This can be used to isolate a badly behaved target on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.25 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517-Q1 supports standard mode as well as fast mode I²C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

Table 9-1. Function Table

| INPUT EN | FUNCTION |
|----------|----------------------------|
| L | Outputs disabled |
| H | SDAA = SDAB SCLA = SCLB |

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

A typical application is shown in [Figure 10-1](#). In this example, the system controller is running on a 3.3 V I²C bus, and the target is connected to a 1.2 V I²C bus. Both buses run at 400 kHz. Controller devices can be placed on either bus.

The TCA9517-Q1 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.25 V bus voltages and 2.7 V to 5.25 V bus voltages.

When the A side of the TCA9517-Q1 is pulled low by a driver on the I²C bus, a comparator detects the falling edge when it goes below $0.3 \times V_{CCA}$ and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517-Q1 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to [Figure 10-3](#) and [Figure 10-4](#). If the bus controller in [Figure 10-1](#) were to write to the target through the TCA9517-Q1, waveforms shown in [Figure 10-3](#) would be observed on the A bus. This looks like a normal I²C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517-Q1, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517-Q1. After the eighth clock pulse, the data line is pulled to the V_{OL} of the target device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517-Q1 for a short delay, while the A-bus side rises above $0.3 \times V_{CCA}$ and then continues high.

10.2 Typical Application

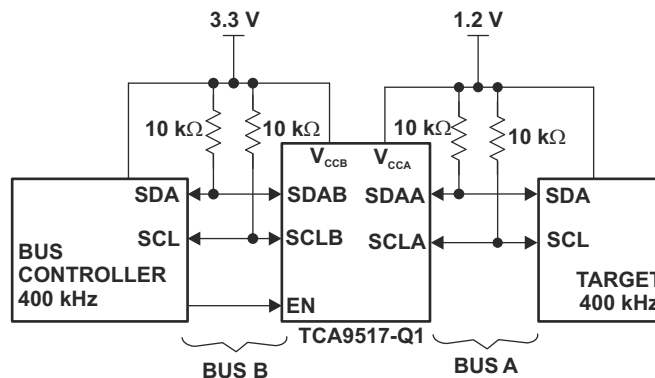


Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

For the level translating application, the following should be true:

- $V_{CCA} = 0.9 \text{ V to } 5.25 \text{ V}$
- $V_{CCB} = 2.7 \text{ to } 5.25 \text{ V}$
- B-side ports must not be connected together

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

10.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517-Q1 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.4 V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

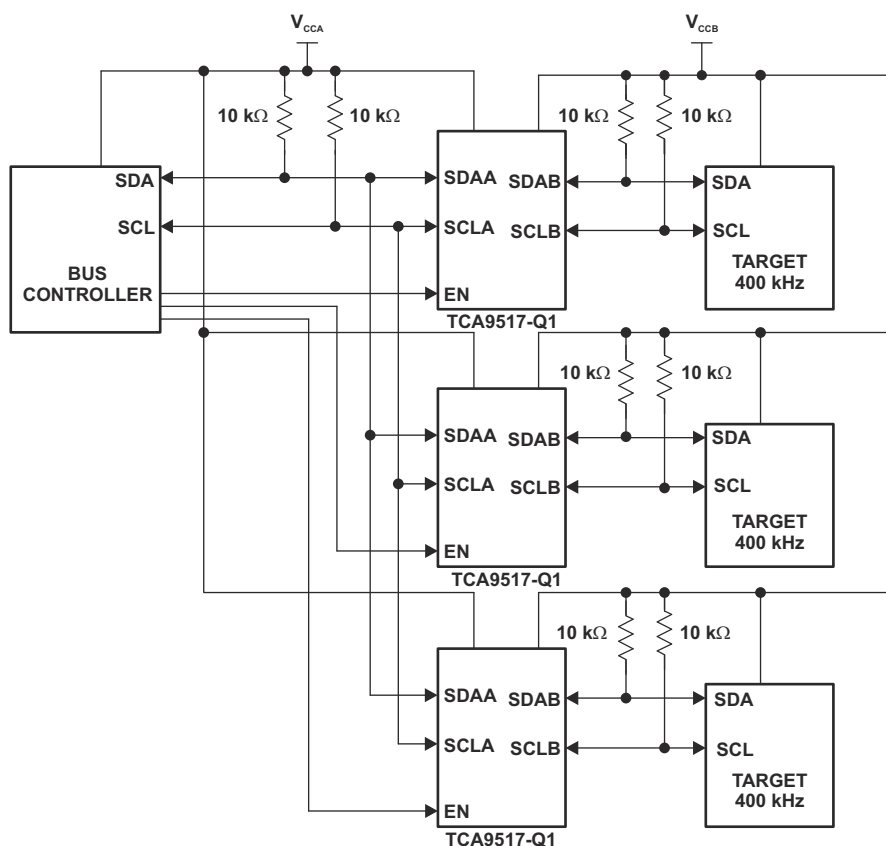


Figure 10-2. Typical Star Application

Multiple A sides of TCA9517-Q1s can be connected in a star configuration, allowing all nodes to communicate with each other.

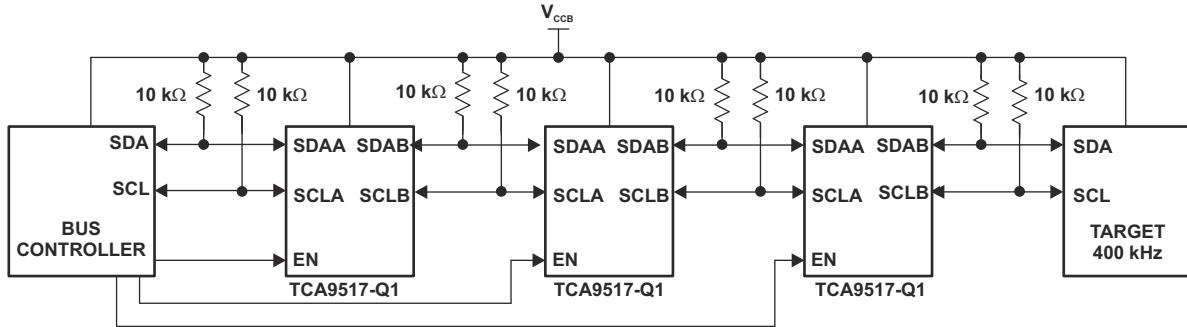


Figure 10-3. Typical Series Application

To further extend the I²C bus for long traces/cables, multiple TCA9517-Q1s can be connected in series as long as the A-side is connected to the B-side. I²C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

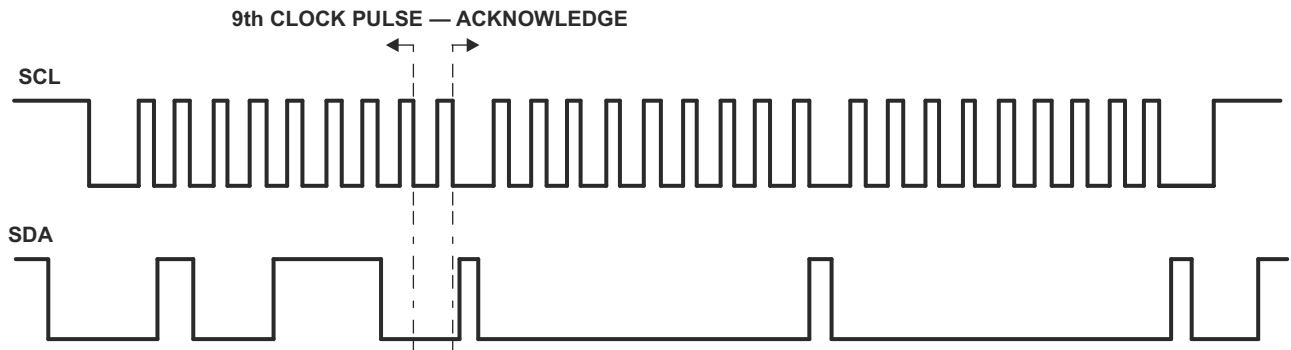


Figure 10-4. Bus A (0.9 V to 5.25 V Bus) Waveform

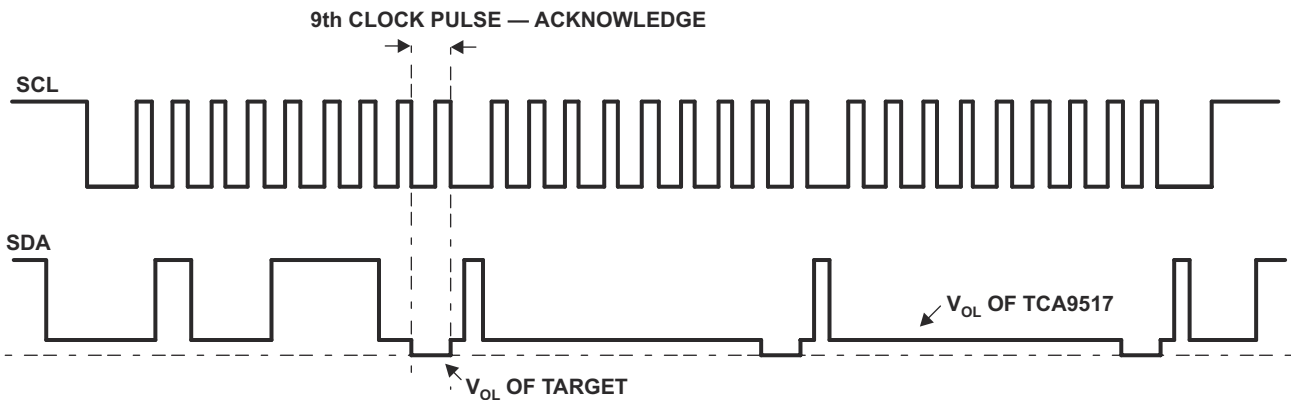
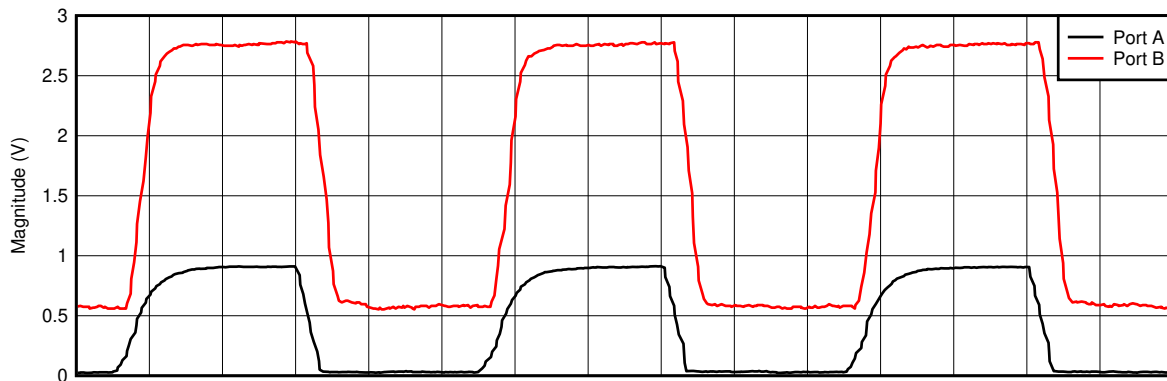


Figure 10-5. Bus B (2.7 V to 5.25 V Bus) Waveform

10.2.3 Application Curve



D003

Figure 10-6. Voltage Translation at 400 kHz, $V_{CCA} = 0.9\text{ V}$, $V_{CCB} = 2.7\text{ V}$

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517-Q1 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the A-side (below $0.3 \times V_{CCA}$) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above $0.3 \times V_{CCA}$, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below $0.3 \times V_{CCB}$, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above $0.7 \times V_{CCB}$. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above $0.3 \times V_{CCA}$.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.

12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517-Q1.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

Figure 12-1 shows an example layout of the DGK package.

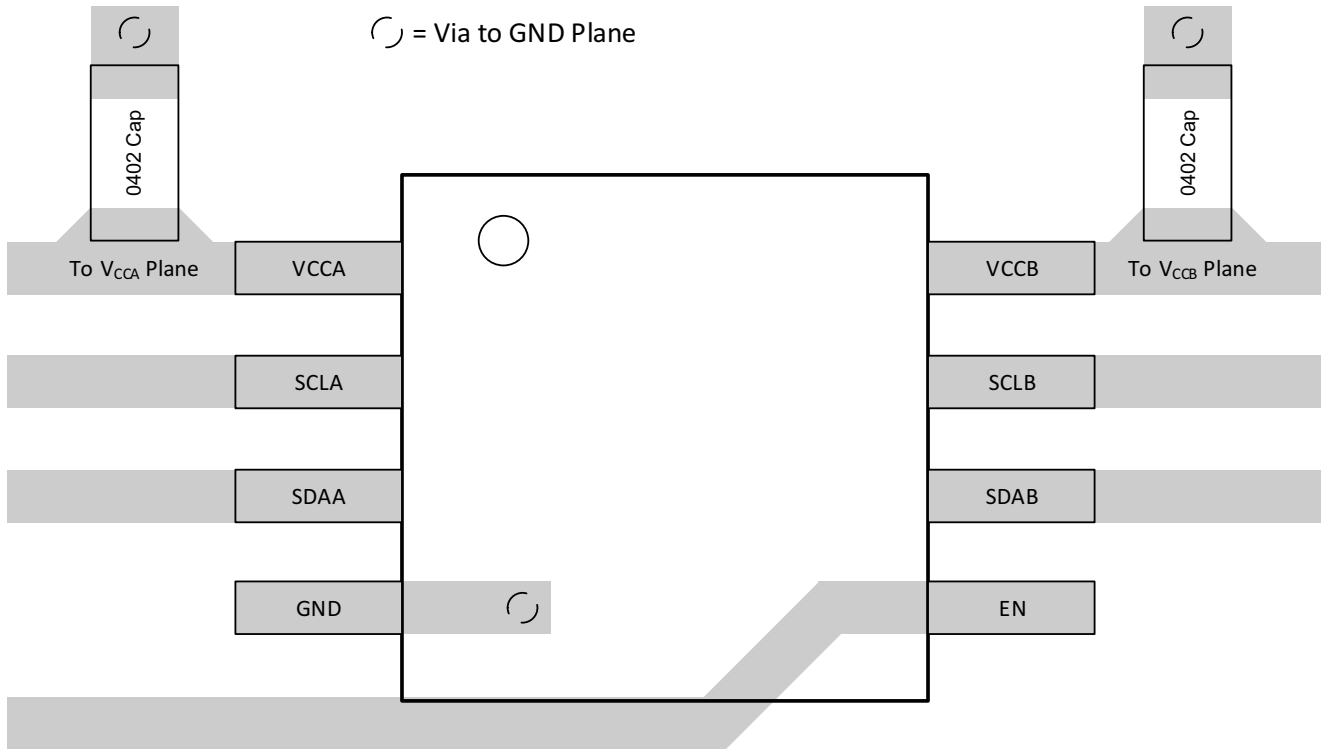


Figure 12-1. TCA9517-Q1A Layout Example

13 Device and Documentation Support

13.1 Device Support

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TCA9517DGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1N2 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TCA9517-Q1 :

- Catalog : [TCA9517](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TCA9517DGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TCA9517DGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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